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A Cascaded NPC/H- Bridge Inverter with Superior Harmonic Content and Improved DC Link Voltage Control for Grid Interface Application

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Abstract: Modeling of Cascaded Multilevel converter has put more emphasize on conventional cascaded H- bridge inverter. First a new phase shifted SPWM control algorithm for cascaded NPC/H-bridge inverter is proposed. Its Superior harmonic suppression is verified by comparing its harmonic spectrum with that of the conventional multicarrier approach. For DC- bus capacitor voltage control, a new, balance circuit is proposed. Because of its modularity, it is simple and can be easily incorporated in cascaded inverter model with any number of levels. Feedback controller design is presented with main focus on grid voltage regulation and overall system capacitor voltage balance. The validity of grid interface model and its control strategies is substantially confirmed by the extensive simulation results.

Keywords: Harmonic Content, Cascaded NPC/H-Bridge Inverter, Grid Connected Systems, DC Link Voltage Control

1. Introduction

The growing attraction of high and medium power applications in utility, industrial and renewable energy systems has increased the demand for high and medium power converters. However due to maximum voltage rating of switches, connecting only one power semiconductor directly to the high voltage is problematic. To address this, a multilevel converter structure has been introduced as an alternative in high and medium voltage applications. Its basic concept is based on the series connection of switching components with several lower DC voltages to synthesize the staircase voltage waveform. Different sources such as capacitors, batteries or renewable energy can be considered as DC sources. Synthesizing a stepped voltage gives better output voltage waveform which is close to sine wave with reduced harmonic content and less *dv/dt* and finally higher output power is easily achieved [1] – [5].

The presented attitudes make the multilevel converter appropriate for various medium and high voltage applications such as has power systems, renewable energy and motor drive systems. Several topologies and control strategies have been proposed for grid interface applications. The commonly used topologies are the high- frequency and line frequency voltage source grid interface system. These topologies employ transformers which come with undesirable features such as increase in cost, size and weight of the whole inverter, also efficiency and reliability of the system is reduced. Transformerless cascaded multilevel inverter is the preferred choice for grid interface applications [6] – [14].

Past research on the model has concentrated on realizing control technique for DC capacitor voltage balance for an output voltage of five levels. This have indicated that is too complicated to balance capacitor voltage for a diode clamped multilevel converter with more than five levels, and is on this basis that this paper presents investigation of a DC- link voltage balance with the use of balance circuit in a single phase diode clamped inverter composed of two three level legs. The proposed technique achieves perfect lower and upper dc link voltage, this combined with the individual voltage control, a complete voltage controller is developed for a cascaded nine level hybrid model. This gives a breakthrough

in realizing DC-voltage balance for multilevel converter with higher voltage levels (more than five).

2. Phase Shifted PWM Control Strategy for a 9-Level Cascaded Hybrid Model Inverter

Based on the Neutral-Point-Clamped (NPC) PWM inverter [15], a new control strategy for cascaded NPC/H-bridge PWM inverter topology is proposed in this thesis. It is shown that a PWM output can be obtained from an inverter leg with a very simple three-level NPC PWM control strategy. The PWM outputs from both legs of the inverter can be combined to form a five-level PWM output [16] with superior harmonic suppression properties. With proper phase shifting of the carriers a further harmonic suppression is achieved for a 9-level voltage output. While other approaches use relatively complicated design procedures, this technique has an advantage of simple design by only changing the phases of the modulating signal and carrier to achieve harmonic suppression. Detailed theoretical analysis of the harmonic characteristics to validate the simulated results has already been done [17]

2.1. Novel Phase Shifting PWM Technique

Figure 1 shows the schematic diagram of the NPC/H-bridge model, which consist of two legs connected to a common bus. The symbol *'p'* and *'n'* denotes the positive and negative rail of the model. Each phase leg is modulated in complementary manner by a carrier/reference comparison circuit. Phase disposition (PD) PWM technique is used as it has superior harmonic suppression in line to line voltage [18]. The figure illustrates the process of generating three level PWM output at leg a and b. The three level PWM output from leg a can be obtained by subtracting v_p from v_n to output voltage V_a as shown in figure 2. The two legs are modulated with 180 degrees opposed reference defined as:

$$\begin{cases} g_a(t) = V_{dc} M \cos(\omega_s t) \\ g_b(t) = V_{dc} M \cos(\omega_s t - \pi) \end{cases} \quad (1)$$

Equation (1) is valid under the assumption that; $V_1 = V_2 = V$ *i.e* the capacitors are balanced.

)

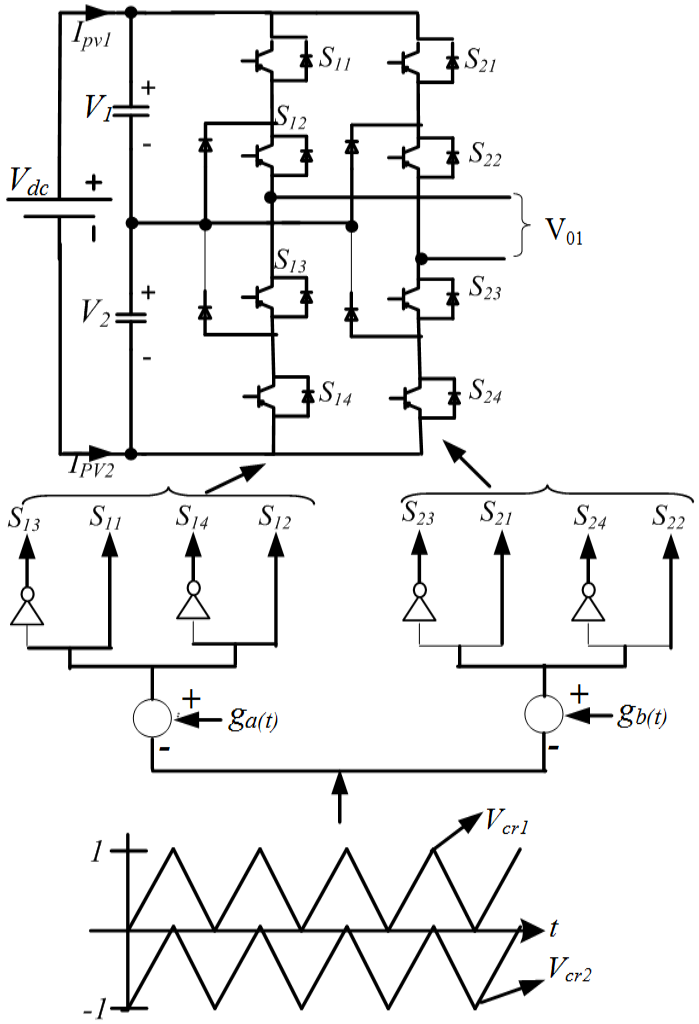


Figure 1. *Schematic diagram of one cell of NPC/H-bridge inverter model and its PWM switching technique.*

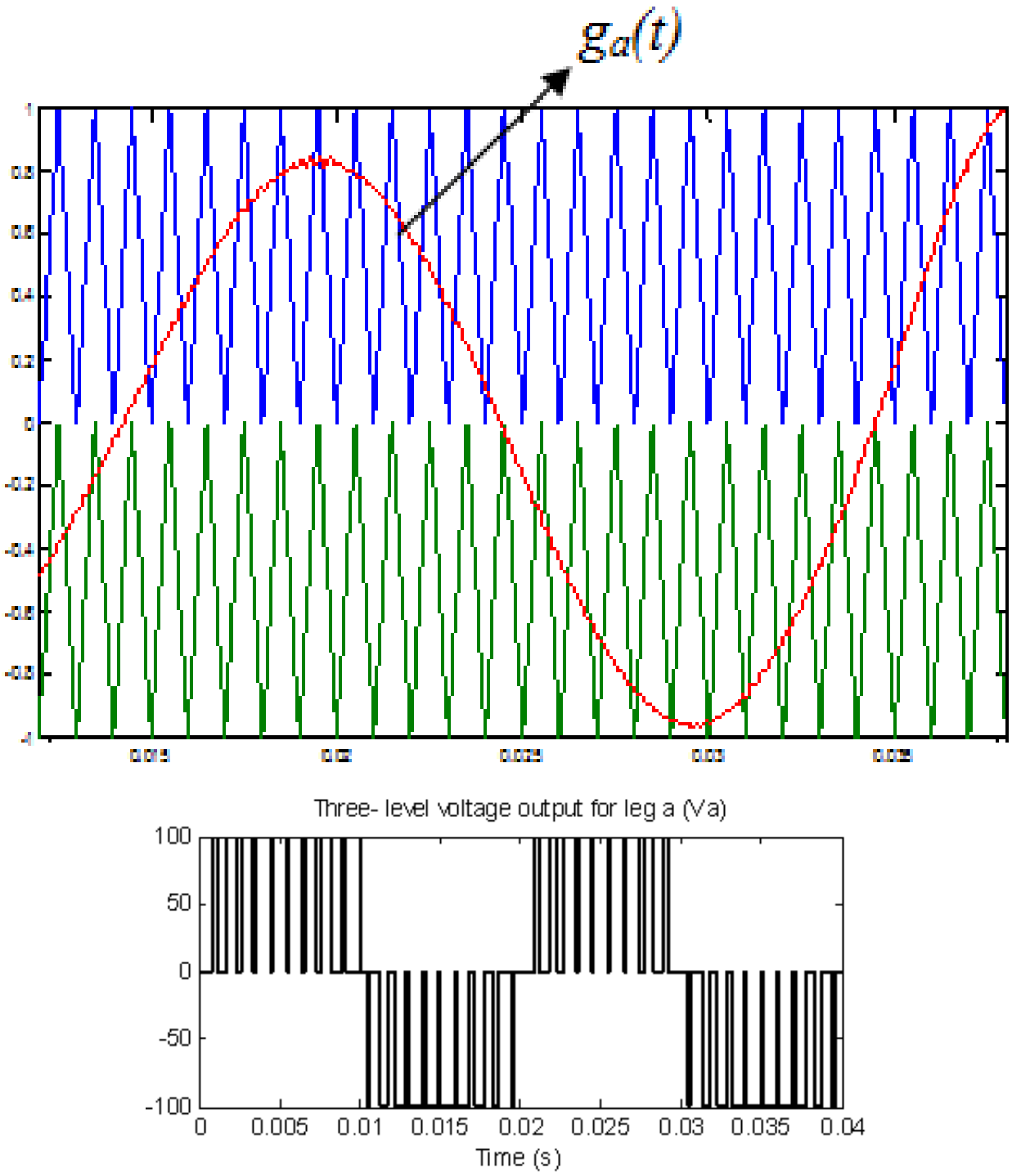
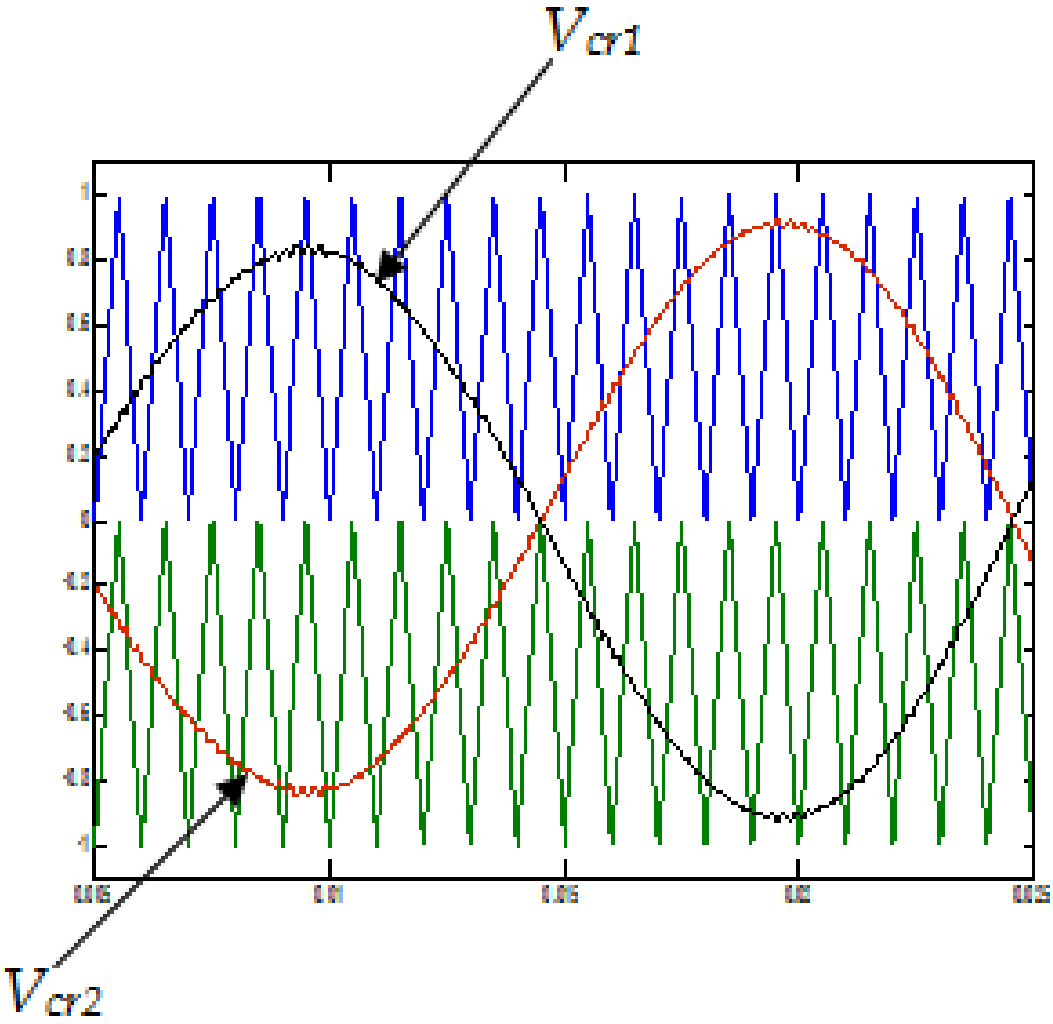


Figure 2. *Control signal and output waveform of leg a.*

Based on the above SPWM technique, an improved phase shifted PWM control strategy is proposed in this thesis. To avoid the complexity of negative and positive legs, the paper uses the principle of decomposition where the whole system is considered as a four cascaded 3-level legs and each leg is treated independently giving three level output. Each two of the four legs are connected back to back and they share the same voltage source V_{dc}. Thus, you need to decompose a 9 - level operation to 4x3 - level sub - operations. PD modulation is used for achieving three level output [9]. Five-level voltage is achieved using two carriers on two three-level legs under PD modulation as shown in Figure 3. By using the same carriers phase shifted by constant value of π/4, a 9- level output is achieved as shown in Figure 4. It should be emphasized that for any number of levels, the two carriers are phase shifted by constant value of π/4. Comparison of the harmonic content of the proposed PWM control with that of conventional multicarrier PWM approach shows that the proposed PWM strategy exhibit superior harmonic suppression as shown in Figure 5.



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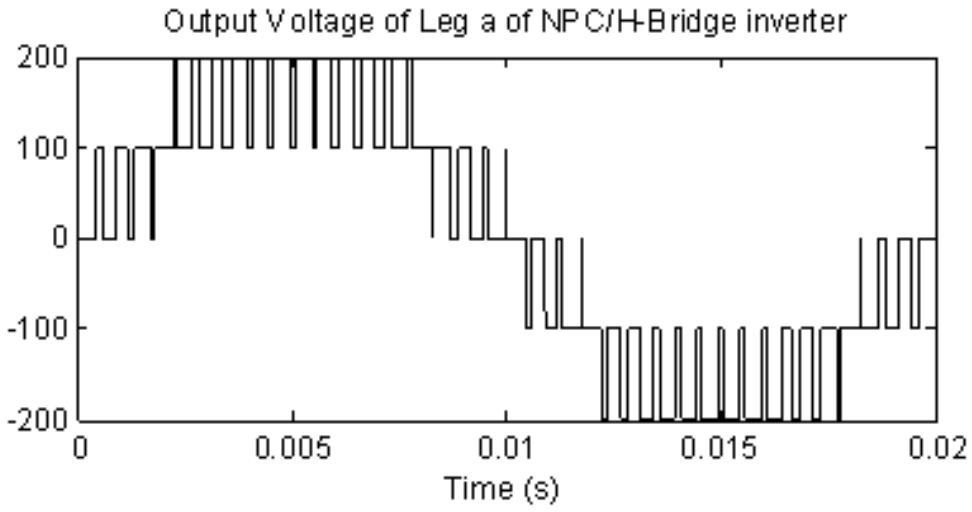
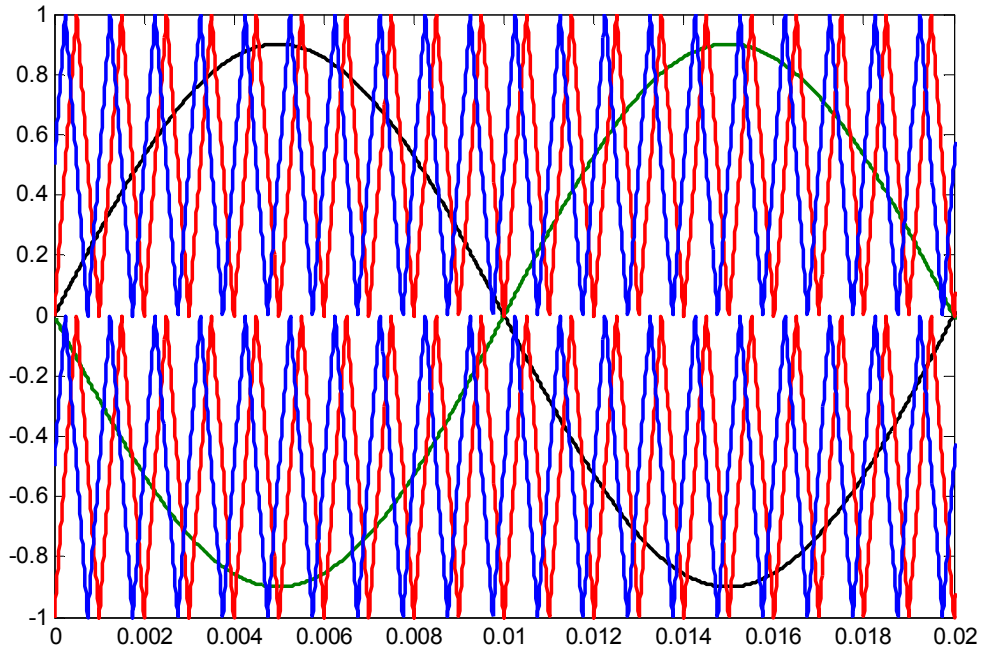
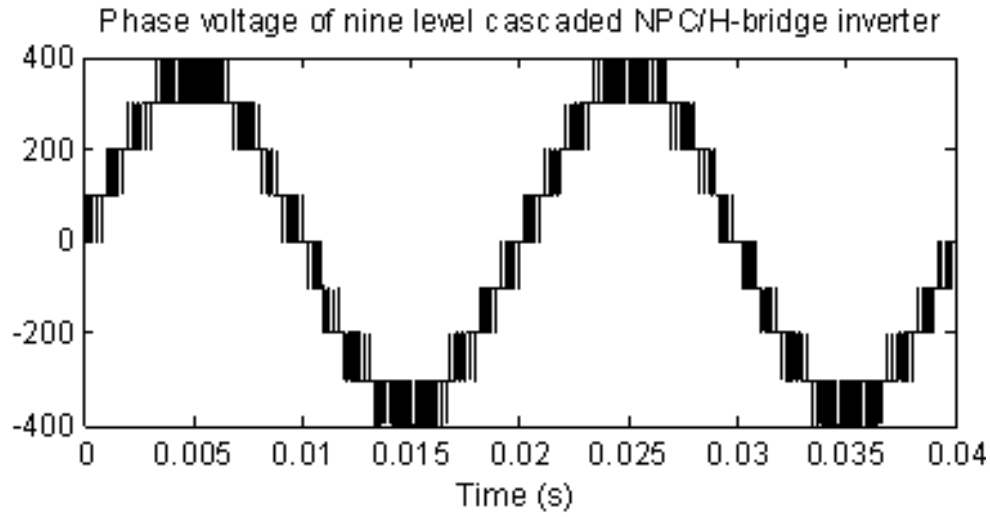


(b)

Figure 3. *(a) PWM scheme and (b) output voltage waveform for one cell of the hybrid inverter.*

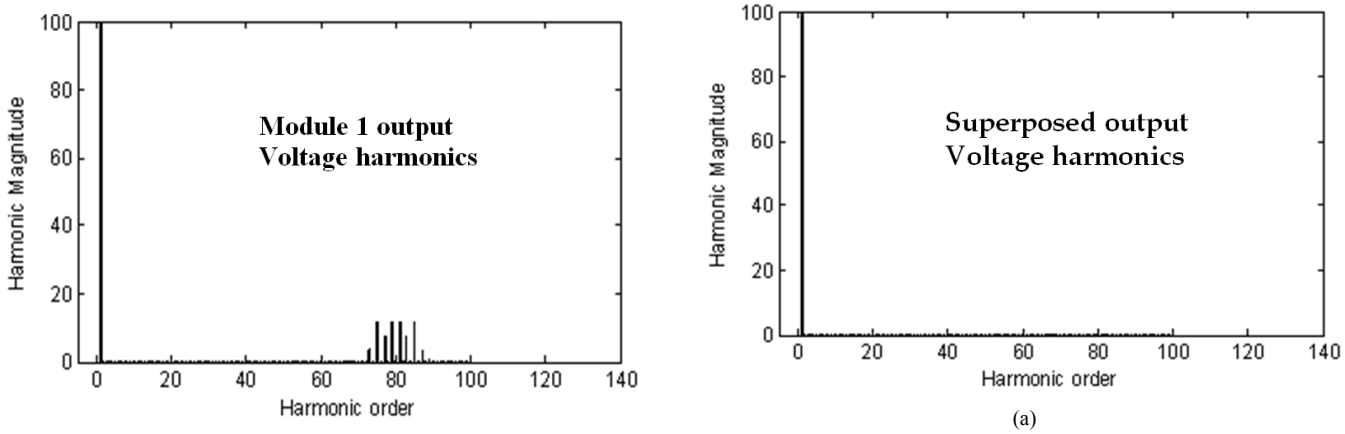


(a)



(b)

Figure 4. *(a) PWM scheme and (b) output voltage waveform for a 9-level hybrid cascaded inverter.*



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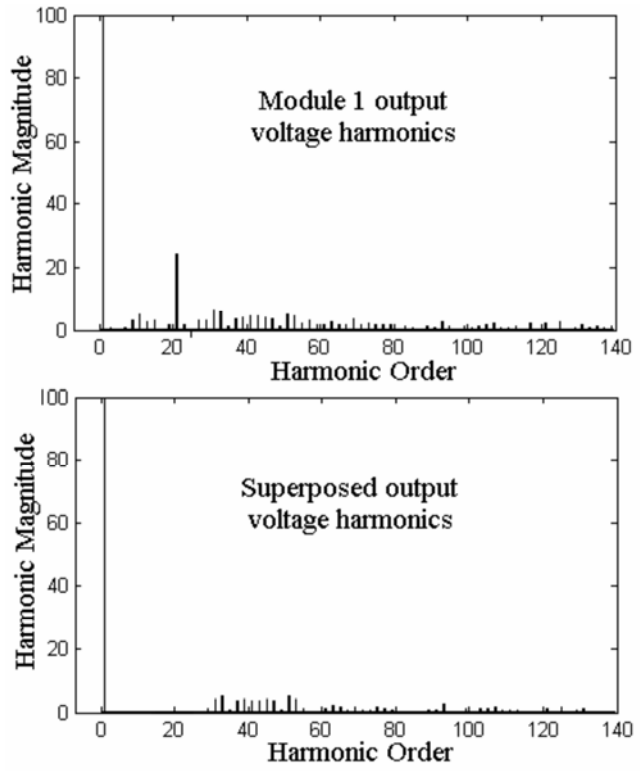


(b)

Figure 5. *Simulation waveforms of hybrid topology using (a) conventional multicarrier phase shifted PWM approach (b) proposed phase shifted PWM approach for both one cell (module) and two-cascaded cells.*

2.2. Principle of Operation of One Cell

To prevent the top and bottom power switched in each inverter leg from conducting at the same time, a control was developed for one cell as shown in Figure 1 by [19] and adopted here for completeness. The constraints of power switches can be expressed as:

$$\left.\begin{aligned} &S_{i1} + S_{i3} = 1 \\ &and \\ &S_{i2} + S_{i4} = 1 \end{aligned}\right\} \tag{2}$$

where i = 1, 2.

Let $T_1 = S_{11}$ & S_{12}, $T_2 = S_{13}$ & S_{13}, $T_3 = S_{21}$ & S_{22} and $T_4 = S_{23}$ & S_{24}. The four valid expressions are given by:

$$T_1 = \begin{cases} 1 \; If \; both \; S_{11} \; \& \; S_{12} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{3}$$

$$T_2 = \begin{cases} 1 \; If \; both \; S_{13} \; \& \; S_{14} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{4}$$

$$T_3 = \begin{cases} 1 \; If \; both \; S_{21} \; \& \; S_{22} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{5}$$

$$T_4 = \begin{cases} 1 \; If \; both \; S_{23} \; \& \; S_{24} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{6}$$

The equivalent switching function in each NPC – leg is given by:

$$K_a = \begin{cases} 1 \quad \text{if } T_1 = 1 \\ 0 \quad \text{if } S_{12} = 1 \\ -1 \text{ if } T_1 = 1 \end{cases} \tag{7}$$

$$K_a = \begin{cases} 1 \quad \text{if } T_3 = 1 \\ 0 \quad \text{if } S_{22} = 1 \\ -1 \text{ if } T_4 = 1 \end{cases} \tag{8}$$

Using equation (3 – 7), a switching state and corresponding voltage output of one cell (five-level inverter) can be generated [16].

3. Converter Control

3.1. Feedback Control Technique

Figure 6 shows a cascaded m-level hybrid inverter model inverter connected to the grid, since the flow of power is always from the dc source to the grid. The system consists of N- DC capacitors, N- inverter cells, LCL filters and the grid. From Figure 6, controller architecture for a nine level cascaded NPC/H-bridge inverter based grid connected systems is designed as shown in Figure 7. The control strategies to be tested are; the grid synchronization using the Phase Locked Loop (PLL); the current reference scheme; the voltage balance technique for lower and upper dc capacitors, individual voltage balance among individual cells and robustness of the dc voltage balance technique under changing loads and changing dc sources.

The phase angles are detected from the grid voltage V_{sa} to perform PLL. As a result sine and cosine terms which are synchronized with the grid voltage are achieved. The obtained current is used as grid reference current for d- channel.

For the grid current control, there are two main control loops, i_{sd} for the active power control and i_{sq} for the reactive power control. The tuning of the compensator is made for only one loop assuming that both of them have the same dynamics. By tracking current signal using current reference generated by the phase voltage of the grid, grid voltage and current are in phase. The aim is to ensure maximum power injection to the grid at unit power factor.

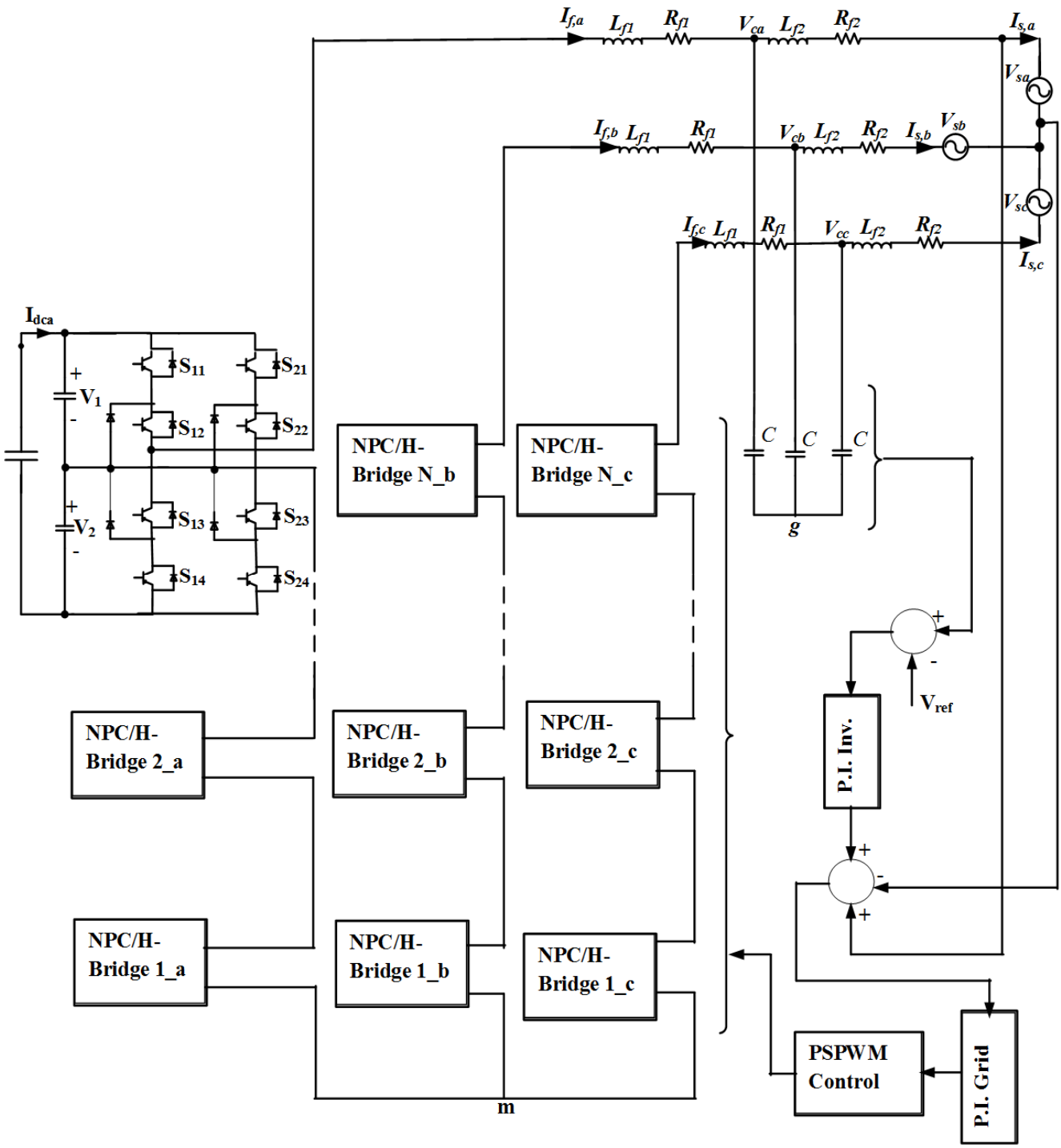


Figure 6. *Schematic diagram of the proposed grid interface system based on N-cascaded hybrid inverter model.*

3.2. Balancing of the DC Capacitor Voltage

A lot of research of research has been done on balancing of DC capacitor voltage for multilevel converter with little success in converters with higher levels (more than five), [20] - [22]. Figure 7 shows a system configuration for a nine level hybrid inverter model equipped with proposed voltage balance circuit per individual capacitor voltage.

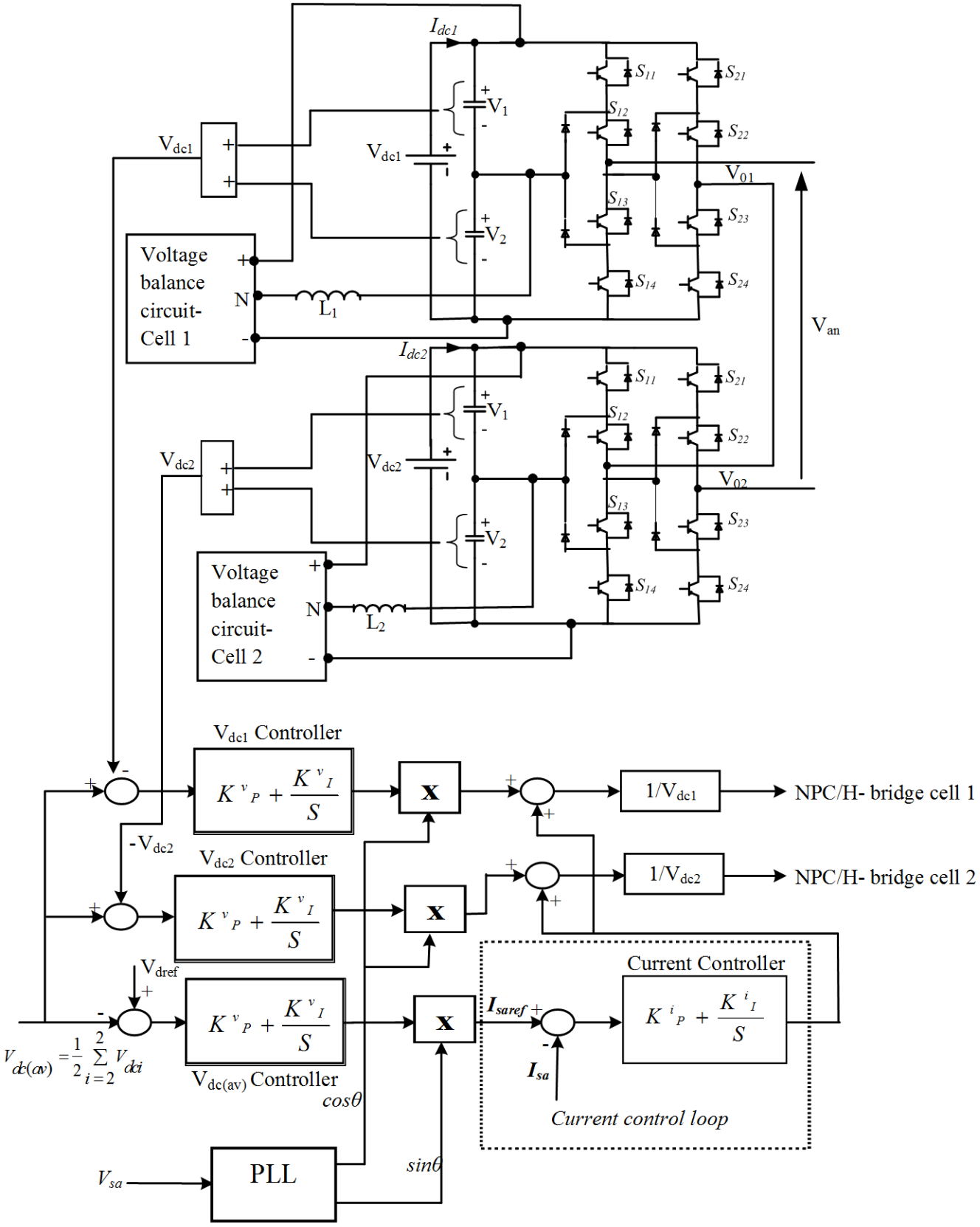


Figure 7. *Control structure of cascaded 9- level hybrid topology.*

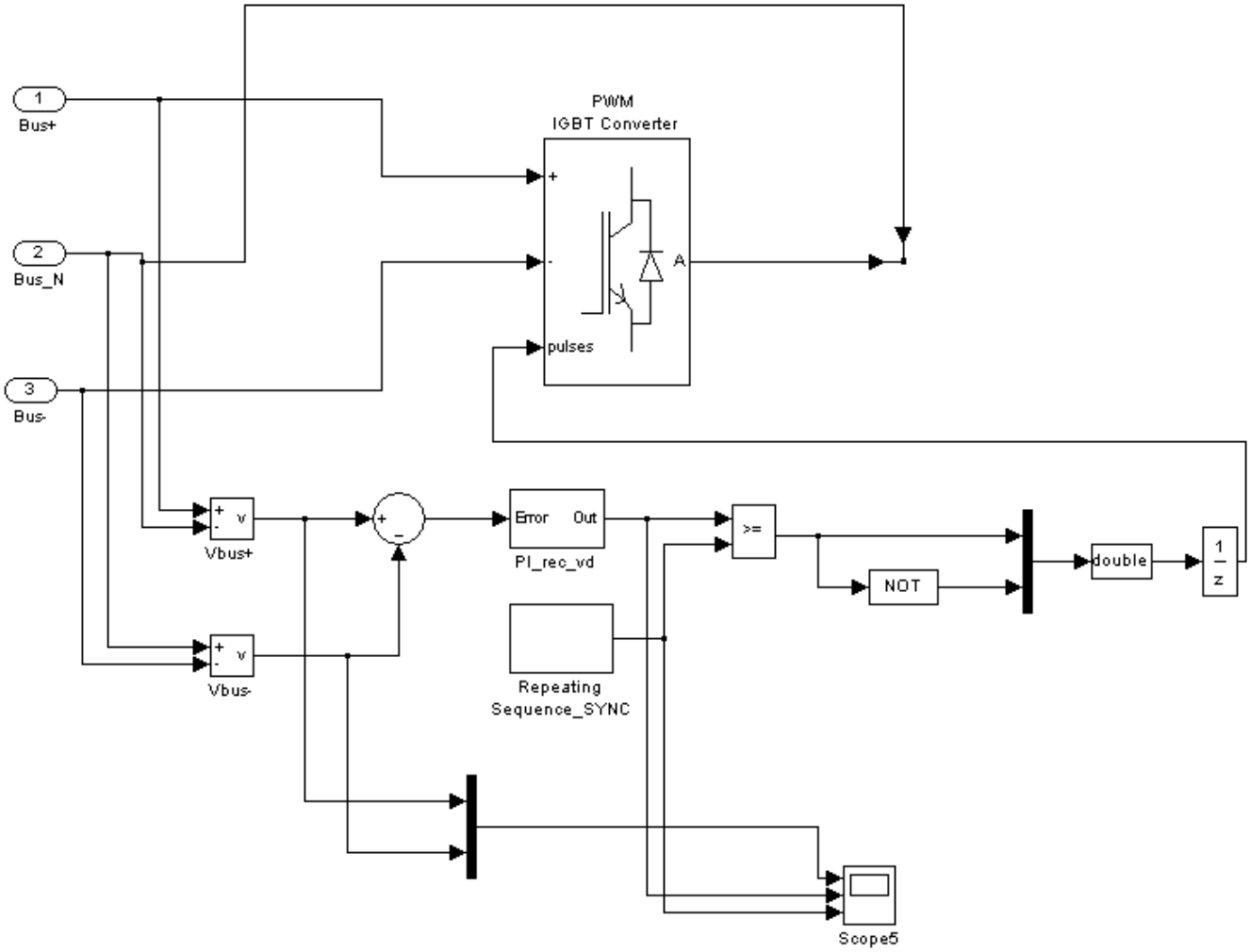


Figure 8. *Voltage Balance circuit for upper (V_1) and lower DC- link capacitor (V_2) per hybrid cell.*

Under normal operation, the average DC capacitor voltage can be controlled by slightly shifting sinusoidal modulating wave of Phase shifted hybrid PWM technique. Thus V_1 of upper capacitor is equal to V_2 of lower capacitor. This implies charging current I_{dc} is symmetrical and current drawn from the neutral point over modulation cycle is zero and neutral potential is constant. But during transient operation or when there is phase to phase imbalance in the output switching pattern, a none- zero neutral current is present, and this means that the charging and discharge of capacitors C_2 and C_1 is not identical. This paper proposes a voltage balancing circuit to correct the deviation (V_1-V_2) in the capacitor voltages as shown in Figure 8. The balance circuit is chosen because it regulates the individual capacitor voltage independently without interfering with other voltage control techniques such as individual voltage control per cell (V_{dc1} and V_{dc1}). In addition it monitors online the deviation in voltages and applies corrective measures by using the same switching frequency.

Since the proposed DC capacitor voltage balance technique utilizes the same voltage balance circuit for upper and lower capacitor voltage balance for N- number of cells, this implies that the technique can easily be applied to control DC capacitor voltage for output voltage levels of more than five which has been a problem to achieve especially for diode clamped multilevel.

3.3. Simulation Analysis of a Cascaded 9- Level NPC/H-Bridge Inverter

To check the validity of the designed small signal model, MATLAB simulation was carried out on the model shown in Figure 9. For the LCL filter Table 1 is as given below. The selection of the type of inductors and capacitors is a compromise between performance, size and cost [23]. The equations describing the operation of voltage and current control loops has been already developed [3]. Therefore for the sake of space, they will not be detailed in this paper, thus the system controller parameters are given in Table 2 for the sake of completeness.

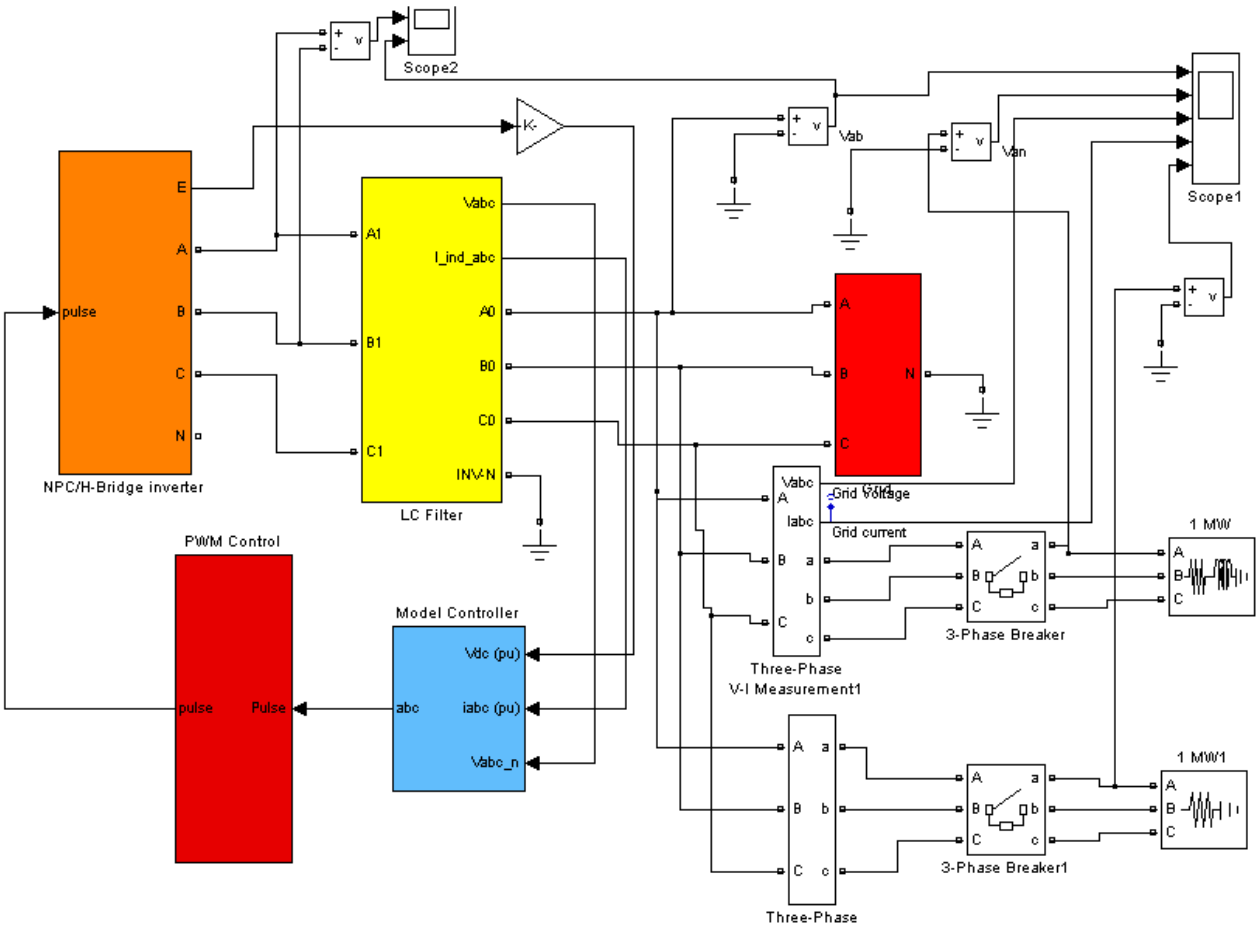


Figure 9. *Complete simulation model of cascaded inverter based grid interface system.*

Table 1. *System component parameter.*

Symbol	Parameter	Value
$V_{s\ x}$	AC source voltage (grid voltage)	600 V, 50 Hz
L_{f1}	Inverter side inductance	0.45 mH
R_{f1}	intern resistance of L_{f2}, inverter side inductance	10 mω
C_f	Filter capacitance	9.4 µF
L_{f2}	Grid side inductance	0.5 mH
R_{f2}	intern resistance of L_{f2}, grid side inductance	1 mω
Rd	Damping resistor in series with C (not shown)	1.6 Ω
C_1=C_2	DC link capacitors	0.042 F

Table 2. *System Controller Parameters.*

Symbol	Parameter	Value
T_{sample}	Sampling period	133 µS
$K^v_{\ P}\_Inv\_Vx$	Voltage control gain (proportional gain)	4
$K^v_{\ P}\_Inv\_Vx$	Voltage control gain (Integral element)	10
$K^i_{\ I}\_Inv\_Ix$	Current control gain (Proportional gain)	0.5
$K^i_{\ I}\_Inv\_Ix$	Current control (Integral element)	20
m_a	Amplitude Modulation	0.9

3.4. Simulation Results and Discussions

The validity and robustness of the proposed control scheme was tested by carrying out several simulations under various environmental conditions. First the model was simulated under normal condition with constant resistive load the Figure 10 shows the grid current and voltage operating under normal condition, it can be seen that a sinusoidal grid voltage that is phase with grid current was achieved by adopting the proposed feedback control technique. This means maximum active power injection into the grid at unit power factor.

For the voltage balance circuit, Figure 6(a) and (b) shows the upper and lower DC link capacitor voltages without the balance circuit first at M = 0.8, then M is reduced to 0.5 and (c) is the capacitor voltages with the balance circuit at both M= 0.5 and 0.8. The model is switched with a steady state load of 200 KW at t = 0.7 sec. This clearly illustrates that one capacitor is charging and another one is discharging this leads to deviation in voltage and hence neutral current which results in distortion of output voltage. It can be seen that the proposed voltage balance works well in the modulation index range of 0.8 to 0.5.

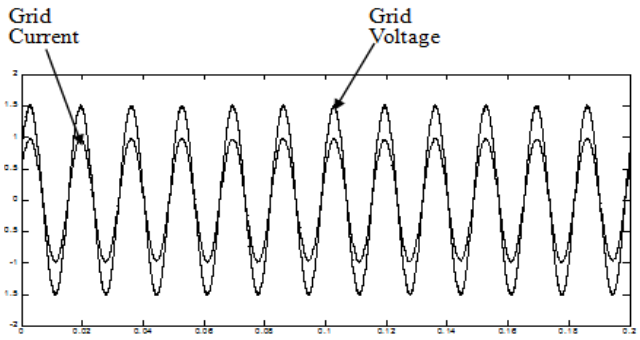
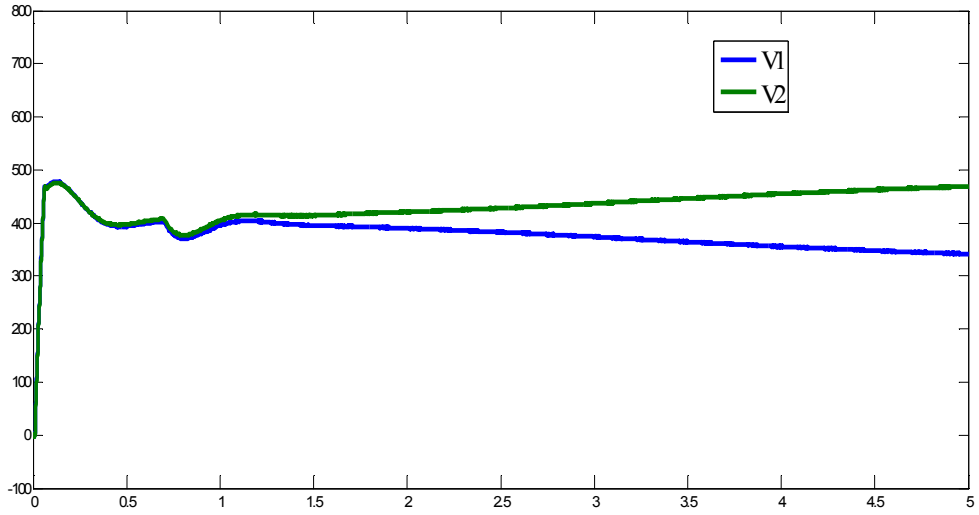


Figure 10. *Grid current and voltage under normal condition.*



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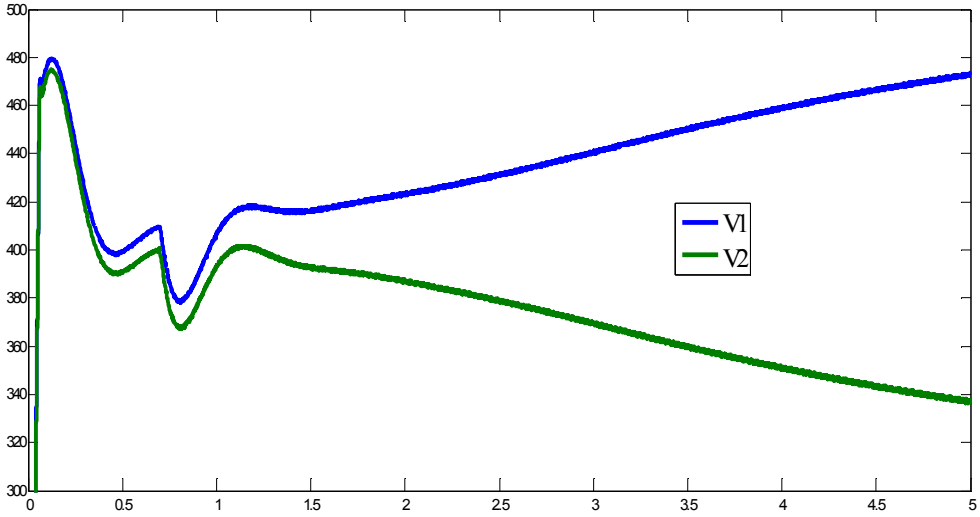

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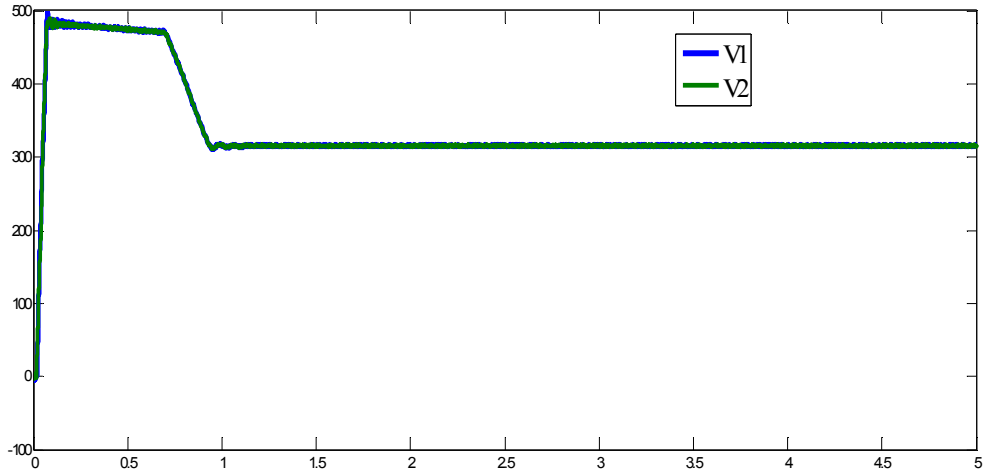
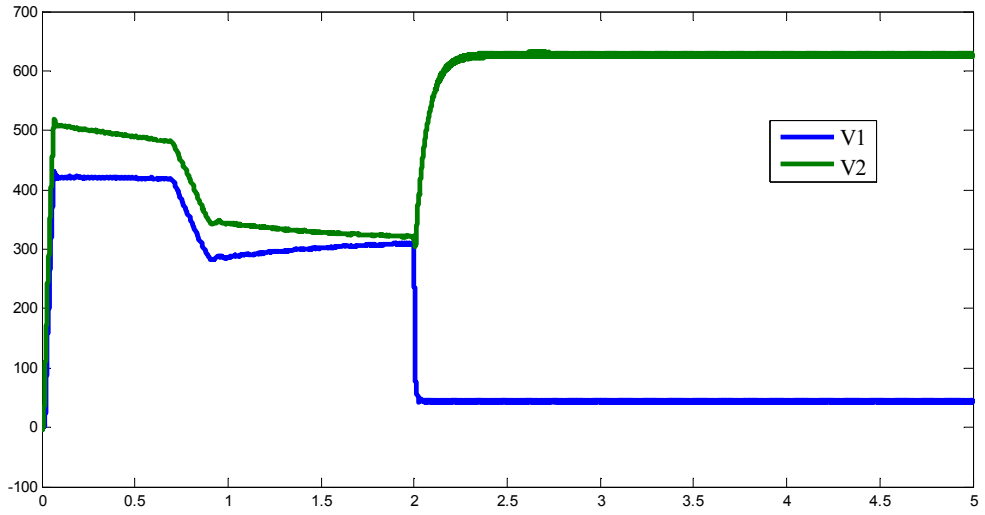


(c)

Figure 11. *Capacitor voltages at normal operating condition (a) without voltage balance for M=0.8 (b) without voltage balance for M=0.5 (c) with voltage balance circuit at both M=0.5 and 0.8.*



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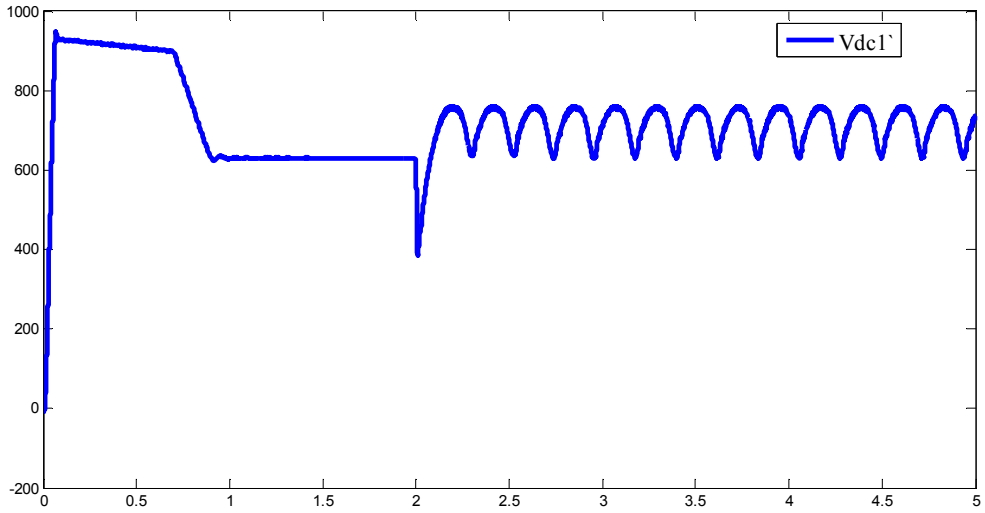

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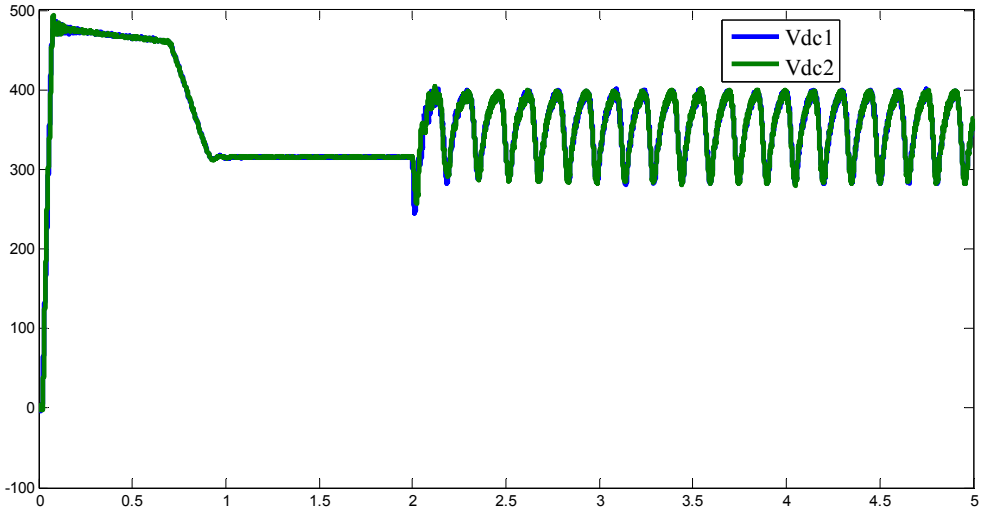
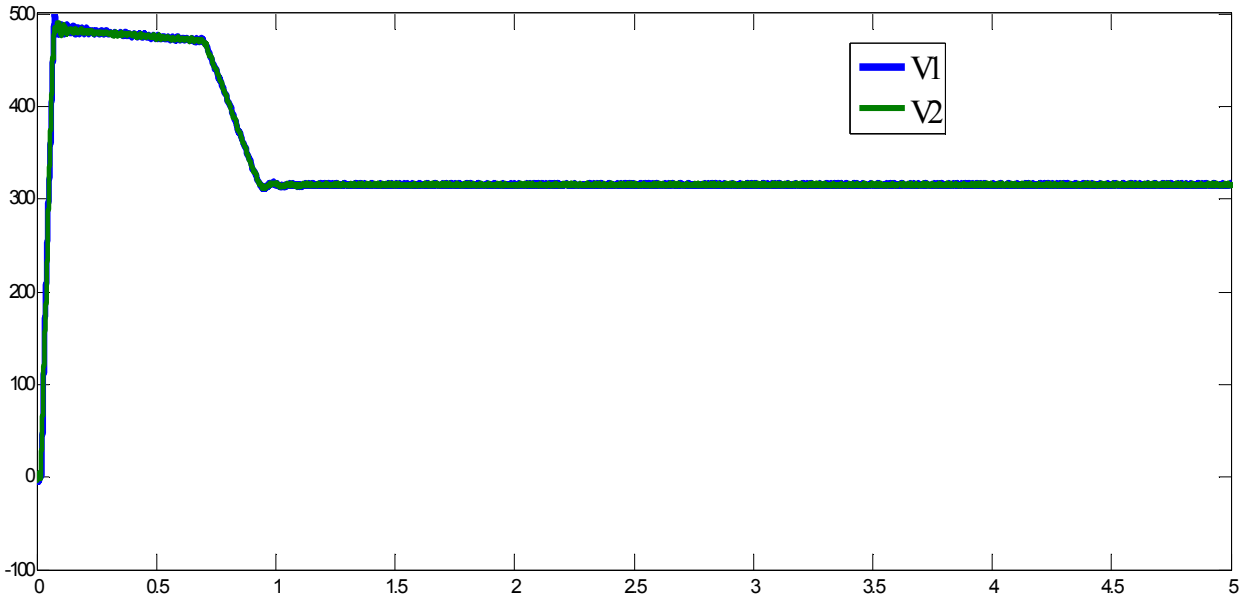


(c)

Figure 12. *Response of the DC link voltages when two different load resistances are connected at t = 2sec. to the upper and lower DC link capacitances (500 Ω to 10 Ω) and lower (500 Ω to 50 Ω). (a) Upper and lower DC link voltages (b) One cell total DC link voltage (c) Two cells total DC link voltages, without voltage balance algorithm.*

To investigate the robustness of the proposed DC-link capacitor balance technique, different resistances at the upper and lower capacitors are used. The resistive load of the upper capacitors changes from 500 Ω to 10 Ω while the lower one changes from 500 Ω to 50 Ω at t = 2sec. Figure 12 (a), (b) and (c) shows the DC link voltage of the upper and the lower DC link voltage, individual cell DC voltage and the two DC link voltages for the two cells respectively with the conventional control scheme, i.e. without the DC link voltage balancing algorithm. Note from Figure 7 there many ripples in the total DC link voltage for the cells V_{dc1} in (b) and also both V_{dc1} and V_{dc2} in (c) due to the distortion in the voltage vector which comes from the unbalance of the upper and lower voltages. The upper DC link voltage reaches 650 V from the normal rating of 500 V. This high voltage can cause serious damage on the devices when the voltage ratings of the DC link capacitors or switches are less than 650 V.

The simulation results with the proposed DC link voltages balancing algorithm are shown in Figure 13 (a), (b) and (c). The lower and upper voltages are balanced well without ripples just as Figure 13 (c) and the total DC link voltage is without voltage distortion.



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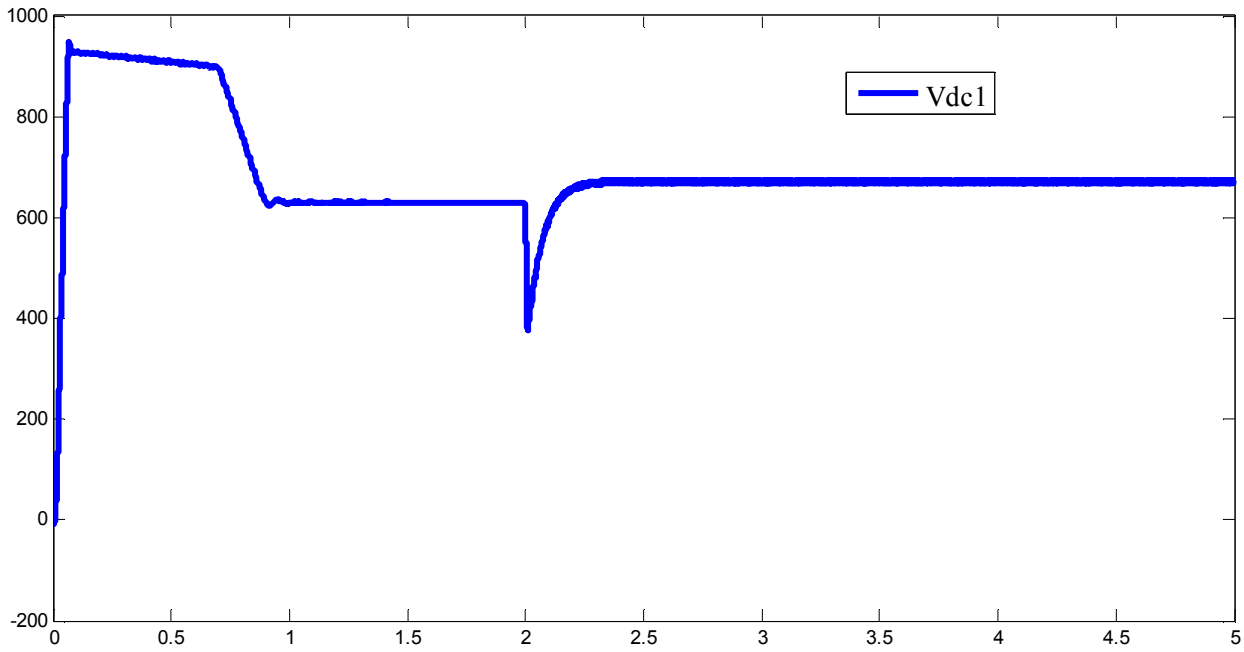

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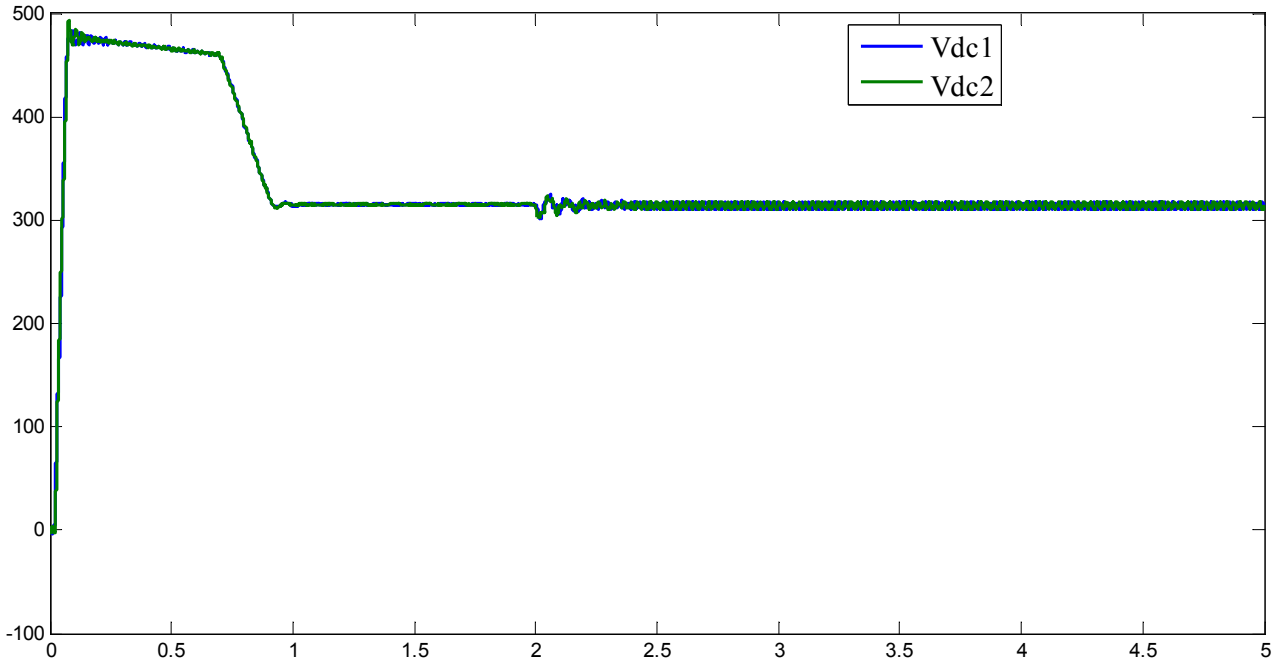
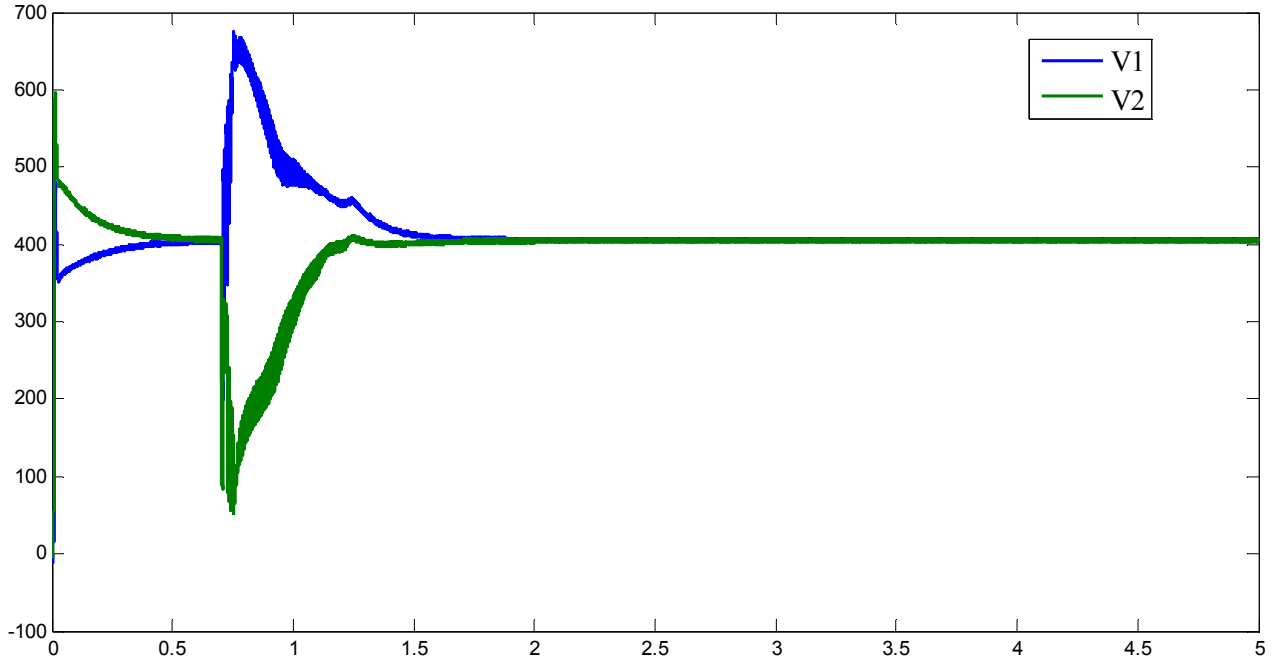


(c)

Figure 13. *Response of the DC link voltages when two different load resistances are connected at t = 2sec. to the upper and lower DC link capacitances (500 Ω to 10 Ω) and lower (500 Ω to 50 Ω). (a) Upper and lower DC link voltages (b) One cell total DC link voltage (c) Two cells total DC link voltages, with voltage balance algorithm.*

Figure 14 (a) shows the effectiveness of the voltage balance circuit per cell and the individual capacitor voltage control for two cells scheme under load perturbations, It can be clearly seen that V_1 and V_2 equals each other in less than 0.03sec., and the DC capacitor voltages V_{dc1} and V_{dc2} in (b) tracks each other shortly after disturbance at t= 0.08s; this is an indication of a well designed voltage controller with fast response.



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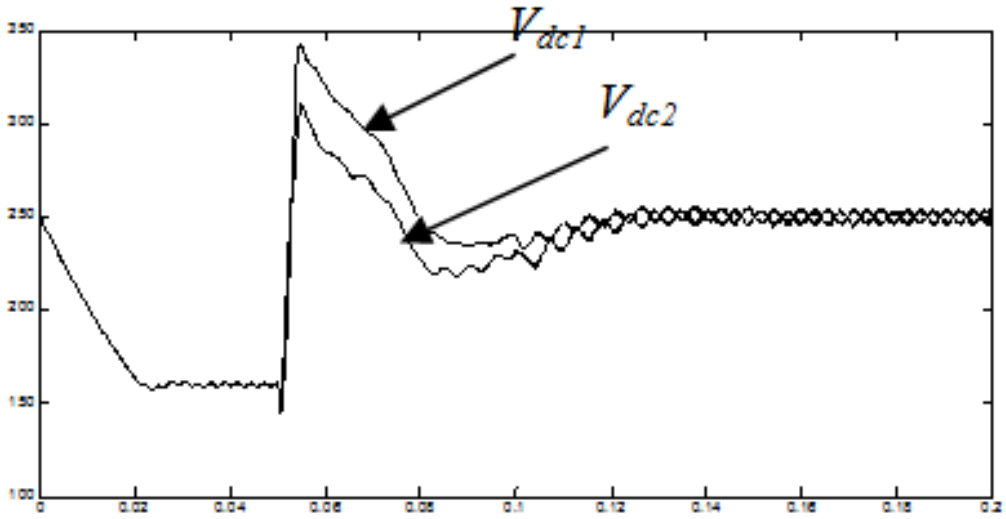
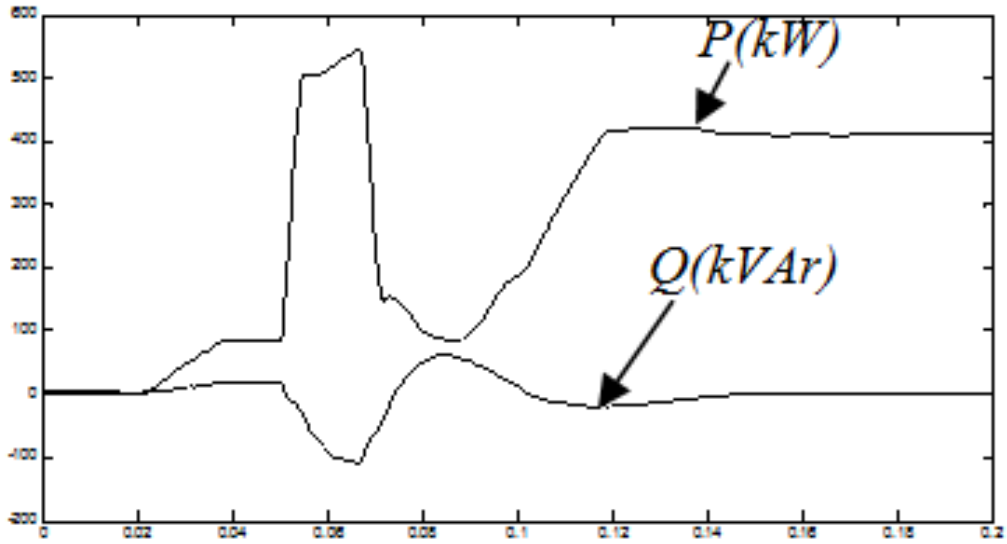


(b)

Figure 14. *Simulation results of (a) V_1 and V_2 (b) V_{dc1} and V_{dc2} due to sudden change of load.*



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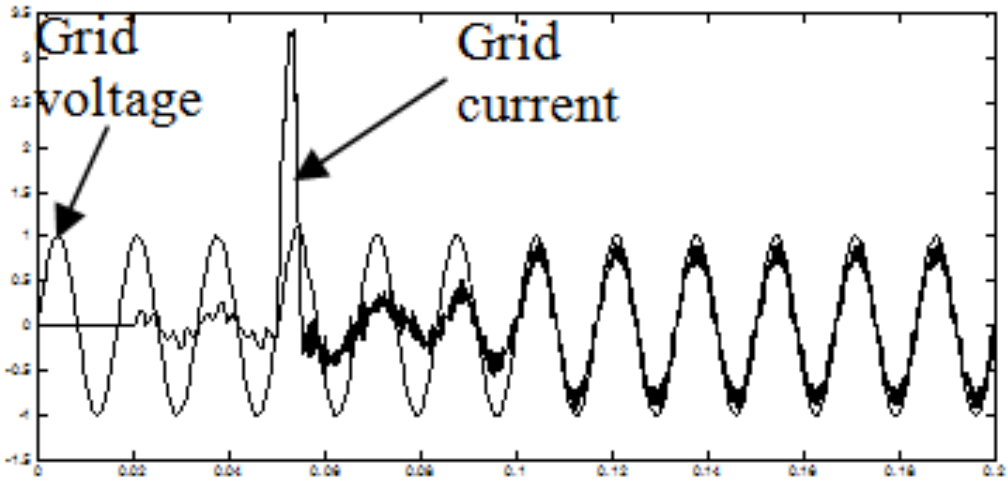

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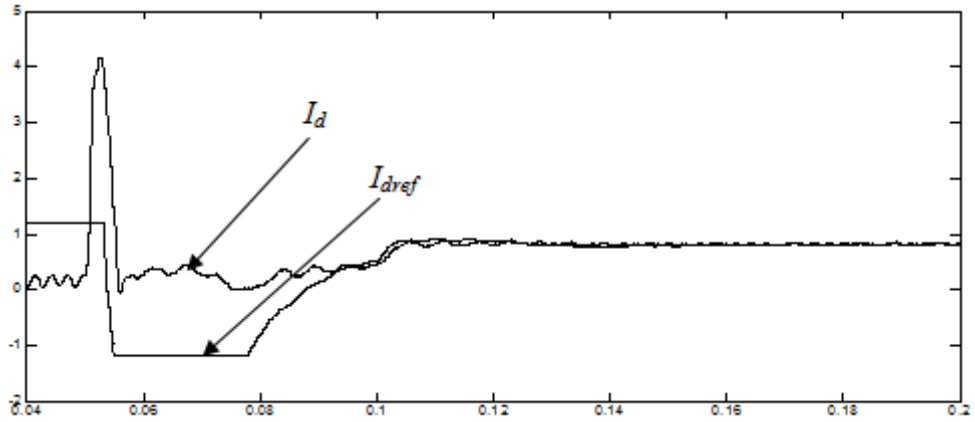

(c)

Figure 15. *Transient simulation of (a) active and reactive power (b) Grid current and voltage due to sudden change of DC voltage (c)) d-q Grid current and their references due to sudden change in the load.*

When the DC bus voltage from the source is perturbed at t = 0.05sec due to sudden increase in load as shown in Figure 14(b), the inverter output voltage is increased making it larger than the grid voltage and thus active power is supplied to the network as shown in Figure 15(a) it is also clearly shown that reactive power is maintained at zero for maximum power transfer from the dc source, this is achieved by setting $i_{qref} = 0$ in 15(d). This change in load at t=0.05 also affects the grid voltage and current but the designed PI regulator forces the grid current to be in phase with the grid voltage after t = 0.08 sec as shown in Figure 15(b). There is good tracking of the *d-q* reference grid current as shown in Figure 15(c).

4. Conclusions

In this paper, It has been demonstrates with proper modeling of the converter, the operating characteristic and the control technique to be applied on the model can be easily found. This can be used to develop standard model for cascaded NPC/H-bridge inverter which is currently not available.

The article has developed an improved topology that can be used to achieve a nine- level NPC/H-Bridge PWM inverter. It has been clearly shown that five level NPC/H-Bridge inverter that has been proposed by many researchers gives a higher THD which is not acceptable in most high and medium power application unless a filter is used. And since there is limited research on cascaded this important hybrid model, the paper has developed a novel phase shifted PWM control technique that was tested on a two cell cascaded hybrid inverter model. In the proposed control technique it has been shown that by properly phase shifting both the modulating wave and the carrier, a nine- level voltage output can be achieved with a reduced harmonic content.

Finally with the proposed simple DC-balance control algorithm, it has been shown that the technique can easily be applied to control DC capacitor voltage for output voltage levels of more than five which has been a problem to achieve in multilevel converters unless a complex technique is adopted. In addition, the robustness of the DC-balance technique clearly shows that control scheme applied on this model is a preferred choice for obtaining a sinusoidal voltage output with a varying DC source (photovoltaic cells).

Nomenclature

a, b	Two NPC/H-Bridge inverter legs
C	Output filter capacitance
C_i	DC- link capacitance for each cell of the hybrid inverter ($C_1 = C_2$)
V_{dci}	DC- bus voltage of the i^{th} cell of the model
f_c	Carrier wave frequency
f_m	Modulating wave frequency
L_{f1}	Inverter filter inductance
L_{f2}	Grid filter inductance
m_a	Amplitude modulation index
N	Number of voltage levels
R_{f1}	Inverter filter leakage resistance
R_{f2}	Grid filter leakage resistance
s	Number of series connected NPC/H-Bridge inverter
V_i	Upper and lower DC link bus voltage for each NPC/H-Bridge inverter ($V_1 = V_2$)
V_g	Grid voltage
x	State vector
ω_s	Target output frequency
M	Modulation Index

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