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# Response mode detection of a linear-logarithmic image sensor using a current–mode readout circuit

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**Abstract:** A current-mode image sensor architecture using a linear-logarithmic pixel in order to improve the dynamic range is presented. The pixel cell is based on a 3T active pixel structure with a PMOS readout transistor in the linear region of operation and a PMOS reset transistor that allows for a linear-logarithmic response. An intrascene dynamic range of 90dB is obtained with a pixel fill factor of 37%. The readout circuit is composed of a first-generation current conveyor, a current memory employed as a delta reset sampling unit, a differential amplifier used as an integrator and a dynamic comparator. The pixel response operating mode is determined in the column readout. A signal is sent to the digital processing unit as an indicator to determine the pixel response operating mode in order to allow the proper analog to digital conversion. The image lag effect observed in the pixel output current is removed by the delta reset sampling circuit. Experimental results, obtained from a test structure, are presented. The circuit was fabricated in a CMOS 0.35um process from Austria Microsystems.

**Keywords:** Active Pixel Sensor (APS), Combined Linear-Logarithmic Response, Delta Reset Sampling (DRS), Current Comparator (CMP)

## 1. Introduction

Image sensors have become a significant silicon technology driver due to the high demand from different applications. In recent years, CMOS image sensors have attracted the attention in the field of electronic imaging. The major reason for the growing interest in CMOS image sensors is customer demand for miniaturized, more integration (more functions on a chip), low power, and cost effective imaging systems [1-2]. The vast majority of the reported image sensors are implemented in voltage-mode [1, 3-6]. Nowadays, size reduction of CMOS devices which necessitates lower supply voltages to reduce the power dissipation has revived interest in current mode techniques. Current-mode operation of various analog circuits is known to offer several advantages, including increased dynamic range, smaller surface, and broad design techniques such as translinear and switched-current circuits. In addition, operation such as addition and subtraction can be more easily implemented in current-mode [7-8]. The quality of an image sensor is largely defined by its dynamic range. As it increases, the sensor can detect a wider range of illuminations and consequently produce images of greater detail and quality. It is impossible to increase the dynamic range by increasing the integration time, because the dark current is integrated in the same way [9]. The logarithmic response CMOS image sensor provides a wide dynamic range using the subthreshold region of a transistor operation. However, at low-illumination levels, their sensitivity is reduced. To alleviate this problem, pixels that combine a logarithmic response at high-illumination with a linear response at low-illumination levels have been designed [10]. Thus, a wide dynamic range is achieved using a combined linear-logarithmic response Active Pixel Sensor (APS). The two modes of operation should be detected in order to apply an appropriate ADC conversion. Current mode imaging structures have suffered from high Fixed Pattern Noise (FPN) due to device parameter variation [11-13]. In a simple 3T pixel structure image lag created by the dependence of the reset photosite voltage on the light intensity also affects the image quality. These variations can be removed at the column readout level by the Delta Reset Sampling (DRS) operation. The basis of this circuit is the switched-current memory cell [14].

Part of this work has been reported in the IEEE NEWCAS conference proceedings [15-16], new key experimental results are presented to complete this work. This paper is organized as follow. Section 2 describes the architecture and

the operation of the imaging system. Section 3 presents the pixel output response without using the DRS circuit. In section 4, the performance of DRS circuit is described. Section 5 presents the mode indicator column readout circuit operation. Finally, section 6 concludes the paper.

## 2. System Architecture and Operation

Figure 1 shows the block diagram of the proposed current-mode imaging system. In the first block, the pixel array is composed of current-mode active pixel sensor having a linear-logarithmic response. In current-mode pixels, the fixed output voltage $V_{ref}$ prevents charging and discharging the column capacitance during readout to maximize the operating speed [11]. The pixel consists of a photodiode, a diode connected transistor $M_1$, transistor $M_2$ operating in the linear region and a row select switch, $M_3$, to connect the pixel to the column bus. The drain voltage of $M_2$ is close to $V_{dd}$ to ensure that $M_2$ operates in the linear region. The voltage $V_s$ determines through transistor $M_1$ the pixel reset and integration phases. The photodiode generates a photocurrent $I_{ph}$ when it is exposed to the incident light during the integration time. The photodiode voltage $V_{pd}$ decreases proportionally to the light intensity and the integration time. This voltage is converted to an output current, $I_{out}$, by transistor $M_2$, acting as a transconductance amplifier. Therefore, $I_{out}$ is linearly proportional to $V_{pd}$. This linearity allows for easy suppression of the fixed-pattern noise using a current-mode DRS at the column circuit.

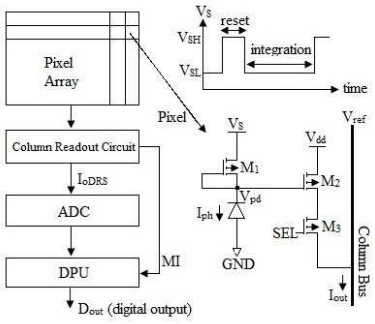



***Figure 1.*** *Imaging System Architecture.*

Figure 2 presents the column readout circuit architecture, being the second block in Figure 1. It is composed of a current conveyor, a DRS circuit, an integrator and a dynamic comparator. The current conveyor generates a fixed voltage node and copies $I_{out}$. The current-mode DRS sends an offset free current, $I_{oDRS}$ to the current mode ADC. The corrected pixel output current is independent of the threshold voltage variations of the pixel readout transistor $M_2$ [12]. The integrator and the dynamic comparator (CMP) determine the operating mode of the pixel which is linear or logarithmic.

The comparator Mode Indicator (MI) indicates to the Digital Processing Unit (DPU) when the pixel is operating in the linear (1) or the logarithmic (0) mode so the ADC output is converted accordingly.

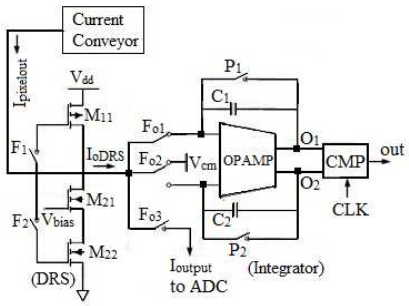



***Figure 2.*** *Column Circuits.*

## 3. Pixel Output Response

Figure 3 shows the experimental results of the pixel response as a function of time with varying light intensities. Increasing the light intensity causes the pixel to reach the logarithmic mode of operation (saturated output current) earlier. It is seen that before saturation, in the linear operating mode of the pixel, the output is not entirely linear. The non-linearity comes mainly from the hole mobility degradation of transistor $M_2$ as a function of $V_{GS}$ and the ''on'' resistance of the select transistor $M_3$. A solution for the non-linearity imposed by the transistor $M_3$ 'on' resistance which results in an increasing drain-source voltage drop as the output current increases, has been proposed in [15] using a digital correction method. The image lag effect shown in Figure 3, due to the dependence of the reset photosite voltage on the light intensity, affects the image quality. For this purpose, the DRS circuit is used as the offset removal circuit. The functionality of the DRS circuit will be explained in the next section.

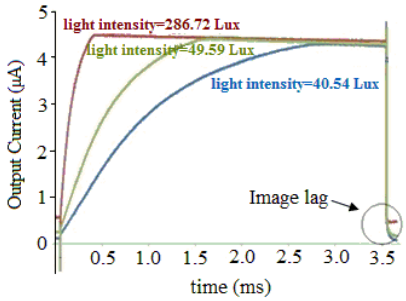



***Figure 3.*** *Experimental results of the pixel output currents.*

## 4. Performance of the DRS Circuit

The delta reset sampling circuit is a current memory cell capable of memorizing the current. It is used in each column to remove the offset current [18].

A light source is used to illuminate the pixel. For each luminance power value, we measure the offset free pixel output current, $I_{oDRS}$. In order to detect a wide range of light intensities, we enable the logarithmic mode of operation by adjusting the low level of $V_S$, $V_{SL}$. It is set to a value so that the pixel can detect high level light intensities. If $V_{SL}$ is set to zero volt, the pixel always works in linear response since

the diode connected transistor, $M_1$, is cut off.

Therefore, for high light intensities, the pixel saturates while it is in linear region and the current will not change by increasing the illumination level.

Figure 4 shows the experimental results of the offset free pixel output current as a function of light intensities for three different VSL. The rate of increasing the output current by light intensity is reduced when the pixel enters into the logarithmic mode of operation. As shown, the pixel enters into the logarithmic mode of operation later for smaller VSL. Therefore, the portion of the linear response of the pixel is greater and also the maximum current reached is larger. The light intensity varies over about five orders of magnitude. Therefore, the pixel intrascene dynamic range measured is about 90 dB. It would be measured further toward high luminance if there were no limitation on the light source.

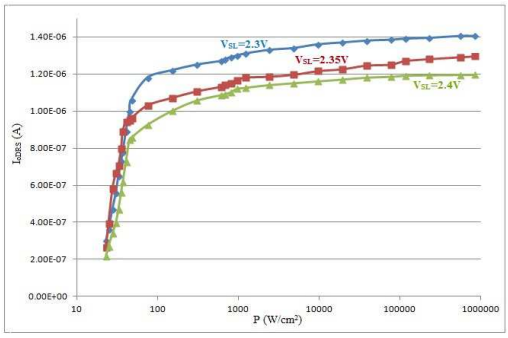
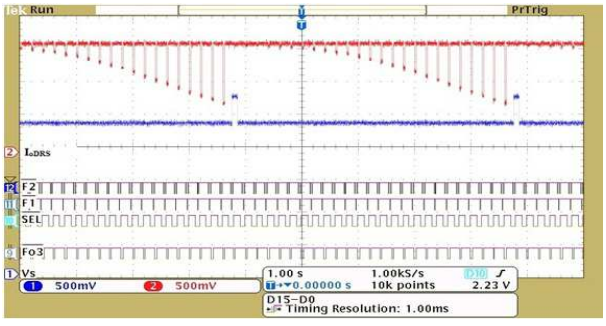
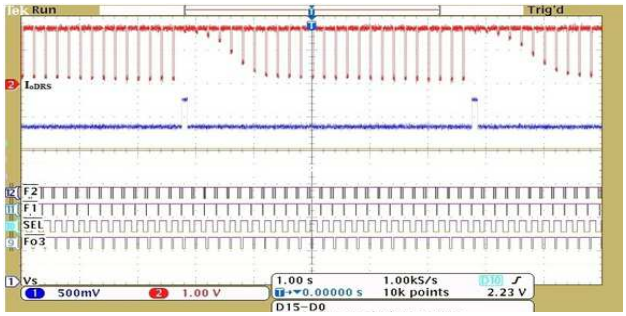



***Figure 4.*** *Measured pixel output current as a function of light intensity for different* $V_{SL}$.

Figure 5 a and b shows the pixel output current, $I_{oDRS}$, sampled by the DRS circuit during the integration time for linear and linear-logarithmic operating mode respectively. As seen, in the linear operating mode, the consecutive samples do not appear linear due mainly to the select transistor "on" resistance and the carrier mobility dependence on the gate voltage. In the linear-logarithmic operating mode, the pixel output current reaches saturation when the logarithmic mode becomes in effect.




**(a)**



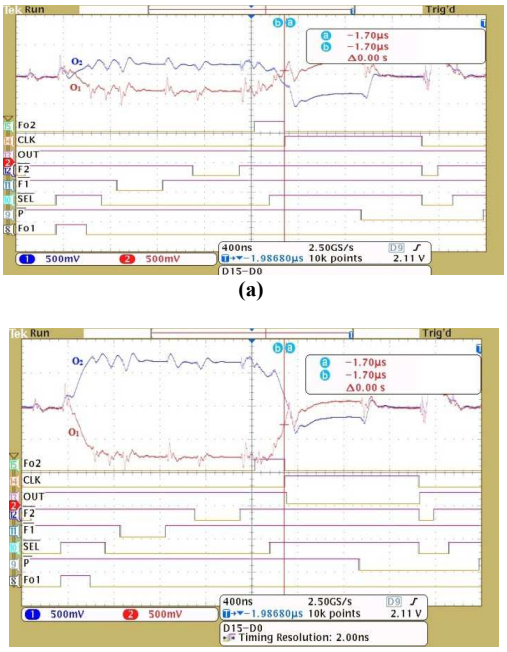

**(b)**

***Figure 5.*** *Sampled DRS output current during integration for a) linear b) linear-logarithmic operating mode.*

# 5. The Mode Indicator Column Circuits

As shown in Figure 2, the mode indicator circuit is composed of an integrator and a dynamic latched comparator which determines the operating mode of the pixel. The integrator is a one stage fully differential amplifier with common mode feedback to control the common mode output voltage [19]. The low power dynamic latched comparator operation has the advantage of having a current flowing only during the regeneration [20-21]. The two outputs of the integrator feed the comparator. The output of the comparator is the mode indicator. According to the pixel response, when it is in the linear operating mode, the two successive currents are different and the first one is smaller than the second one. So, the comparator output should be "1". However, in the logarithmic mode of operation, the comparator output changes to "0" since two consecutive $I_{oDRS}$ readout would be nearly identical [16].

The timing diagrams and measured inputs and output of the dynamic comparator are shown in Figure 6 a and b. F1 and F2 are the input switches of the DRS as shown in Figure 2, while Fo1 and Fo2 are its output switches. In Figure 6a, since the light intensity is low, the pixel works in linear mode. Therefore, after performing the DRS, the first sampled current is smaller than the second one. In these conditions, the voltage variation related to $O_2$ is larger than the one of $O_1$. This happens during the regeneration process of the comparator, when the CLK signal is high. In this case the pixel operates in linear mode. The result in Figure 6 b, for high light level, shows the pixel operating in logarithmic mode. Therefore, when the CLK signal is high, during the regeneration phase of the comparator, the comparator output turns to "0" since $O_1$ is smaller than $O_2$. The regeneration finishes when the CLK signal is low and the comparator is reset. The switches P1 and P2 reset the capacitors before starting the output phases, so the inputs and outputs of the integrator are on a common mode voltage level.




**(a)**

**(b)**

***Figure 6.*** *Experimental results obtained from the integrator and the dyamic comparator for a) the linear and b) the logarithmic mode of the pixel response.*

In this work, the pixel circuit uses a linear-logarithmic response to provide a high dynamic range in current-mode operation from a simple 3T APS architecture. The results of the proposed pixel and the existing CMOS APS pixels are compared in Table 1. As shown, the voltage-mode APS presents a higher dynamic range at the expense of a more complex architecture, taking up a larger area. It is seen that in current-mode APS, the dynamic ranges are low since the simple pixel architecture is working only in the linear region. Compared to the other pixels in this Table, the proposed pixel is compact, works in current-mode and shows a fairly high dynamic range due to the combined linear-logarithmic pixel response.

***Table 1.*** *Pixel performance comparison.*

| Reference | Pixel Operating Mode | Pixel Response | CMOS Technology | Pixel type and Architechture | Dynamic Range (In trascene) |
|---|---|---|---|---|---|
| [13] | Voltage- Mode | Linear-Logarithmic | 0.35 µm 2P4M, 3.3V | 5Tr - APS | 112 dB |
| [22] | | Logarithmic | 0.35 µm 1P5M, 3.3V | 5Tr with comparator-A PS | 137dB with variable integration time |
| [23] | | Logarithmic | 0.25 µm | 4Tr - APS | 137 dB |
| [24] | | Logarithmic | 0.25 µm | 5Tr combining the lateral PNP - APS | 120 dB |
| [25] | | Logarithmic | 0.5 µm | 5T - APS | 120 dB |
| [26] | | Linear | 0.18 µm 2P3M | 6 Tr- APS | 94 dB with two exposures |
| [11] | | Linear | 0.35 µm 2P4M, 3.3V | 3Tr - APS | 64 dB |
| [27] | Current- Mode | Linear | 0.25 µm, 2.5 V | 1.5Tr - APS | 63 dB |
| | | | | 3Tr - APS | 58.3 dB |
| This work | | Linear-Logarithmic | 0.35 µm 2P4M, 3.3V | 3Tr - APS | 90 dB |

# 6. Conclusion

The current mode combined linear-logarithmic response pixel provides a high dynamic range of about 90dB. The design of this CMOS image sensor with a three transistor pixel includes many analog circuit blocks such as the current conveyor, the current memory cell, the fully differential integrator and the dynamic latched comparator. Based on our analyses, we have proposed some new idea to improve the circuits such as a column level pixel operating mode detection, and an improved current memory precision. More specifically, the new 3T architecture active pixel design has the advantage of both current-mode operation and linear-logarithmic APS response. We have chosen a fully differential amplifier with a dynamic comparator to determine the working mode of the pixel. The result is sent to the digital processing unit so that the ADC digital output is converted accordingly. The experimental results obtained from the fabricated prototype are measured on a single active pixel sensor with a fill factor of 37%.

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