CMOL Based Quaded Transistor NAND Gate Building Block of Robust Nano Architecture

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Abstract: Nano architectures are more prone to defects. This work is aimed at finding the effectiveness of using quaded structure devices to improve the reliability of logic gates in Nano level. Transistor level redundancy (Quaded Structure) has been applied in a CMOS gate (NAND) design to improve the reliability. Being an universal gate, NAND gate can be the building block for nano architecture. CMOL is a hybrid architecture that combines conventional CMOS and Nano architecture together. Based on CMOL, a NAND gate design has been proposed. To study the performance of the proposed architecture, theoretical analysis has been proposed. Moreover, to evaluate the effectiveness of the quaded structured NAND (QNAND) gate, detailed simulation was carried out. Simulation results illustrates that quaded structured design achieves significantly higher defect tolerance by enhancing the reliability of the QNAND gate.

Keywords: Quaded Structure, Reliability, Cmol, Nand Gate, Nano Architecture

1. Introduction

Nano+Micro hybrid architecture is an integration of nanowire crossbars with CMOS circuits. This hybrid architecture provides ultra-dense integration of devices and interconnects. So the performance with respect to speed, power and area, is superior to nano or micro architecture alone. CMOL ("CMOS + NANOWIRES + MOLECULES") developed by Likharev et. al [1], combine CMOS logic elements with nanowire crossbar arrays similar to Field Programmable Gate Arrays (FPGA).

In nano scale, there are uncertainties due to inherent characteristics of the devices, stochastic nature of fabrication process and external disturbance. These uncertainties are the source of faults in nano level. Popular self assembly fabrication processes have probabilistic nature which result in a fairly large percentage of defective devices. Due to small cross section areas of wires, they become fragile. Moreover, the contact area between nanowires and between nanowires and devices depends on a few atomic-scale bonds. For these reason, some connections become poor and effectively unusable [2, 3, 4]. In

comparison with the failure rate of conventional CMOS (approximately $10^{-7} - 10^{-6}$), the failure rates of nano scale devices are just under unity. These devices are more sensitive to external disturbances, such as radiation effects, electromagnetic influence, parameter fluctuations, and high temperatures. In addition, process variations introduced due to uncertainty and complexity of nanoscale device fabrication process can affect leakage dissipation, power consumption, reliability, and defect [5, 6, 7]. Hence permanent and transient [8] faults or defects will occur during the manufacturing phase and during the field operation due to such factors as aging, while transient faults will appear in the field due to external disturbances.

Redundancy-based defect tolerance techniques can tolerate against both permanent and transient faults. [15] proposesan architecture for a silicon-based quantum computer processor based entirely on complementary metal-oxide semiconductor (CMOS) technology, which is the basis for all modern processor chips. Redundancy can be added at the transistor level, gate level or functional block level. If the most fundamental component of a design (i.e. transistor) are made more robust by using redundancy,

it will improve the design reliability more when compared with defect tolerance techniques applied at higher level of abstraction (block level or functional level). Adding redundancy at the transistor level is less costly in terms of overhead when compared with the same defect tolerance techniques applied at higher level (block or functional). Adding redundancy at lower level of the design abstraction is a promising technique and merits further consideration and research. [16] presents a Single Event Upset (SEU) robust low phase-noise PLL for clock generation in harsh environments like nuclear and space applications. The PLL has been implemented in a 65 nm CMOS technology. [17] introduces a new approach to design fault-se-cure encoder and decoder circuitry for memory designs. The key novel contribution of this paper is identifying and defining a new class of error-correcting codes whose redundancy makes the design of fault-secure detectors (FSD) particularly simple. [18] develops a complete synthesis and performance optimization methodology for switching nano-crossbar arrays that leads to the design and construction of an emerging nanocomputer.

2. Theory of CMOL Based Quaded Transistor

2.1. Quadded Transistor Structure

Defect tolerance can be improved by adding redundancy at

transistor level. In Quadded Transistor logic each transistor of a circuit is replaced by a quadded transistor structure as shown in figure 1(b), (c).

Single transistor defect: Transistor defects are expressed as stuck-open, stuck-short, bridge between gates etc. Any single transistor defect can be tolerated by quadded transistor structure implementing either the logic function (A+A) (A+A) or the logic function (AA) + (AA) as shown in figure 1(b), 1(c). For nMOS transistor, OR-bridge and stuck-short defects produce the same behavior while the AND-bridge and stuck-open defects have same behavior. Similarly, for PMOS transistors, OR-bridge and stuck-open defects produce the same behavior while AND-bridge and stuck short defects have the same behavior.

If the defects do not occur in any two parallel transistors, T_1 & T_2 or T_3 & T_4 for figure 1(b), double stuck open or their corresponding bridge defects are tolerated. Double–stuck short or their corresponding bridge defects are tolerated as long as they do not occur to any series transistors T_1 & T_3, T_1 & T_4, T_2 & T_3, T_2 & T_4 for the figure 1(b), and T_1 & T_3 or T_2 & T_4 for figure 1(c).

Triple Defect: Triple defects are tolerated if those defects are not in parallel as two stuck-open or are not in series as two stuck-short defects or their corresponding bridging defects.
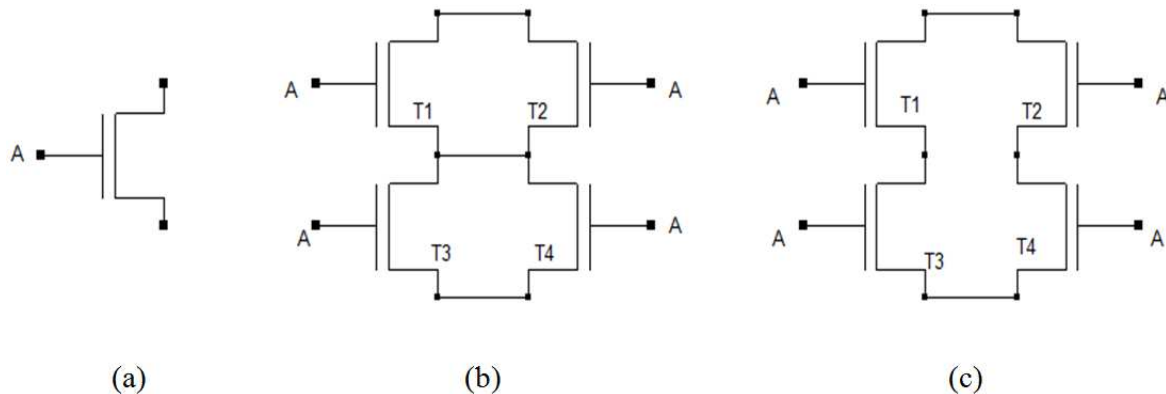

Figure 1. Quaded Transistor Structure.

2.2. CMOL Circuit Architecture

The basic idea of CMOL circuits is to combine the CMOS technology with molecular-scale two-terminal nano devices. The advantages of CMOS are its flexibility and high fabrication yield. The nano devices have extremely high potential density. CMOL fabrication costs may be at affordable level due to relatively large critical dimensions of CMOS components and the "bottom-up" approach to nano device fabrication. At the same time, the density of active devices in CMOL circuits may be as high as 10^{12} per cm^2 and that they may provide an unparalleled information processing performance, up to 10^{20} operations per cm^2 per second, at manageable power consumption.

CMOL circuits consist of two levels of nanowires. At each cross point of a "crossbar" array, Nano devices are formed by

self-assembling (figure 2). The CMOS/nanodevice interface problems are overcome in CMOL circuits by providing interface pins that are distributed all over the circuit area, on the top of the CMOS stack. (Silicon-based technology necessary for fabrication of pins with nanometer-scale tips has been already developed in the context of field-emission arrays [9].) As Figure 1c shows, There are two types of pin, reaching to either the lower or the upper nanowire level. Pins of each type are arranged into a square array with side 2 βF_{CMOS}. Here F_{CMOS} is called the half-pitch of the CMOS subsystem. B is a dimensionless factor whose value is larger than 1 and it depends on the CMOS cell complexity. The nanowire crossbar is turned by angle $\alpha = \arcsin (F_{nano}/\beta F_{CMOS})$ relative to the CMOS pin array, where F_{nano} is the nano wiring half-pitch [10].

Two nanowires which have contact with two pins may be

connected to CMOS data lines by activating two pairs of perpendicular CMOS lines, (figure 2b). As Figure 1c illustrates, this approach allows a unique access to any nano device, even if $F_{nano} \ll F_{CMOS}$ [10].
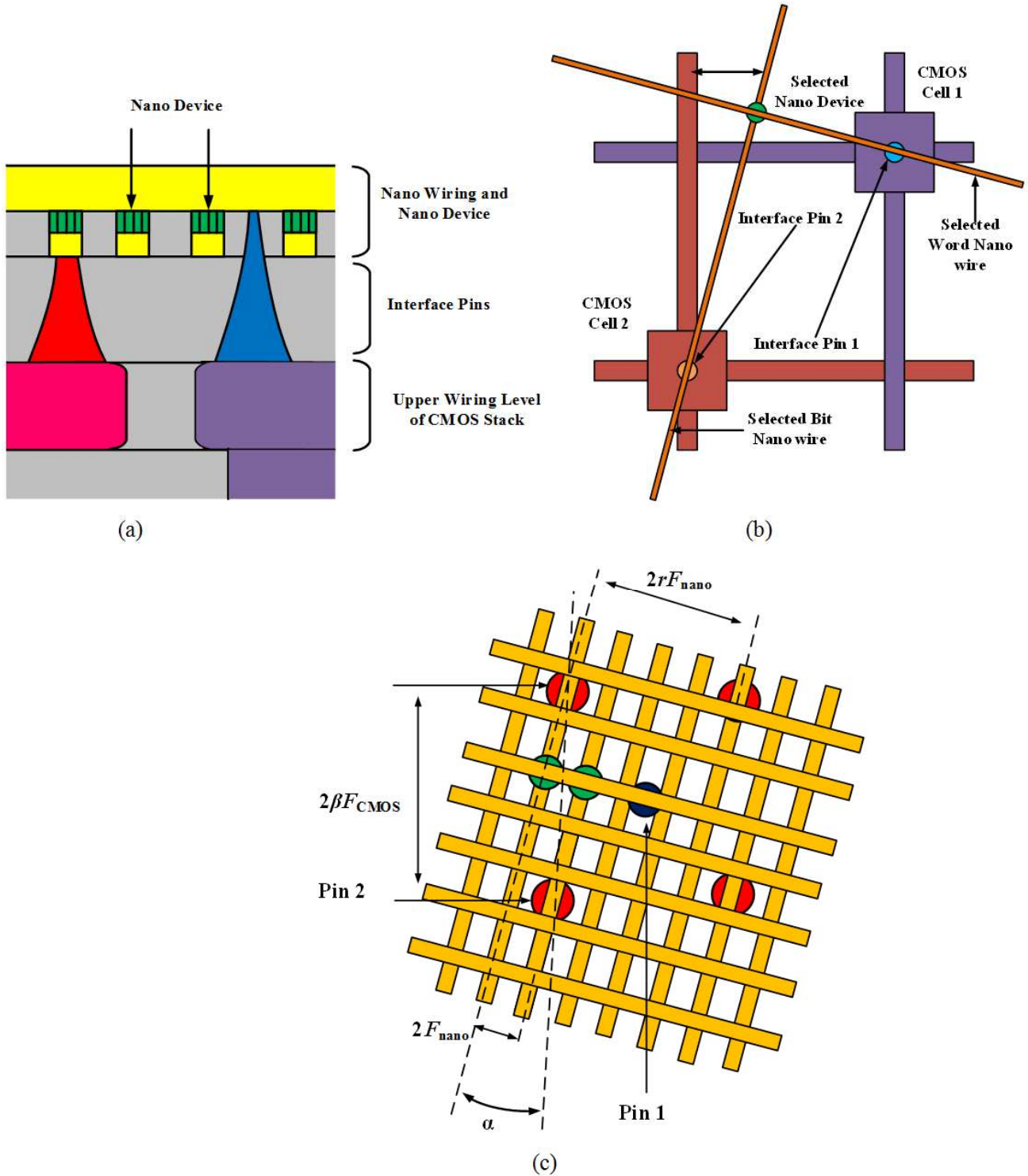

(a)

(b)

(c)

Figure 2. The generic CMOL Circuit [10].

3. Configuration by CMOL FPGA

Strukov described the configuration of simple NOR gate by CMOL FPGA [11]. CMOS inverters together with pass transistor and nano devices were used to form the basic 'wired-NOR' gates (figure 3). The pass transistors were used as pull-down resistors, while the nano devices set into ON (low-esistive) state were used as pull-up resistors. For example, if only the two nano devices shown in figure 3(b) are in the ON state, while all other latches connected to the input nanowire of cell F are in the OFF (high resistance) state, then cell F calculates the NOR function of signals A and B [11].
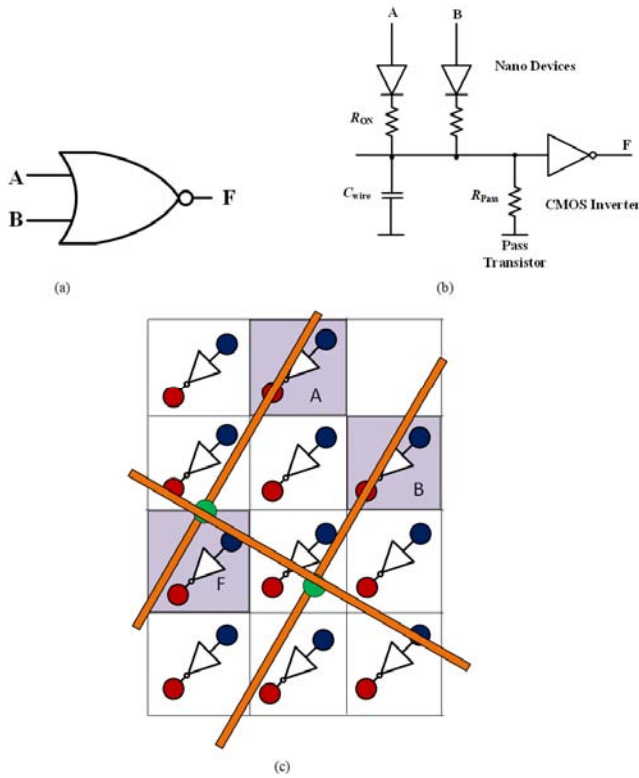
Figure 3. CMOL wired-NOR gate: (b) Schematic and (c) One of (many possible) CMOL configuration.

3.1. Proposed Configuration of NAND Gate

Similarly we proposed the configuration of CMOL based NAND gate. If any one of the nano devices are in OFF (high resistance) state, then cell F calculates the NAND function of signals A and B figure 4.
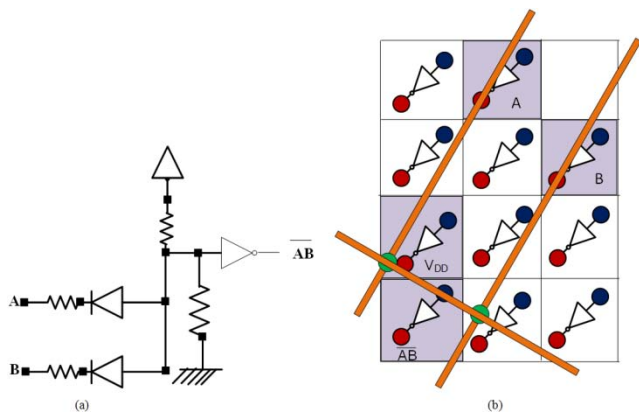

Figure 4. Proposed configuration of CMOL based NAND gate. (a) Schematic and (b) One of (many possible) configuration.

3.2. Electrical Model of the Proposed Configuration

According to Strukov's model [11], nanowires within a layer are separated by a distance equal to their width. Let the nanowire width is 15 nm, a switching layer separating the two nanowire layers is 3 nm thick and there is an insulator between and around all nanowires with a dielectric constant of 3.9 (that of SiO_2). Then according to the Strukov's model we can

predict a capacitance per length of approximately 2.8 pF cm^{-1}. We can choose a material having a lower dielectric constant around 3.5 as a passivation layer covering the top nanowire layer that protects the nanowire layers. Nanowire pads add additional capacitance that can be neglected since their area is quite small compared to that of the nanowires. From these considerations we can estimate the nanowire capacitance at 2.0 pF cm^{-1} [11].

The effective resistivity of the the nanowire material decides the resistance per unit length of nanowire. According to Strukov's model, we also assume here that the nanowirers are copper nanowirers (the metal specified in the ITRS roadmap). For example, Cu wires with a line width of 15 nm are projected to have an effective resistivity of approximately 8 $\mu\Omega$ cm, so a square Cu nanowire, 15 nm on a side, would have a resistance of about 355Ω μm^{-1}.

It is difficult to model nanowire resistivity, ρ, for very small (<10 nm) wires. A common approximation by Strukov [11] was

$$\rho/\rho 0 = 1 + 0.75(1 - p)(\lambda/d) \qquad (1)$$

Here

p is the fraction of electrons scattered specularly at the surface and is assumed to be 0.67,

λ (the mean free path) is equal to 40 nm,

ρ_0 (the bulk resistivity) is equal to 2 $\mu\Omega$ cm, and

d is set to the nanowire width.

But this model does not reflect properly the effective resistivity for small wires [12] and assumes negligible increased resistivity due to scattering at grain boundaries (which is possible for very large grain sizes). According to Snider [13] we fitted the resulting model to the ITRS resistivity model, finding a reasonable fit for $p = 0.6$ and a grain boundary reflectivity coefficient of 0.43. For 30 nm pitch nanowires, we have chosen closed-junction resistance value as 24 kΩ.

The projected n-FET switching time was 0.39 ps for the year 2010 from the ITRS roadmap [14]. Accordingly the CMOS gate delay was estimated t 10 ps. Circuit timing is strongly dominated by the RC delays of the nanowires.

According to Strukov's model [11] the average total power consumption of a CMOL gate may be estimated as a sum of

Static power P_{ON} due to currents I_{ON},

$$P_{ON} \approx \frac{V_{DD}^2}{2R_{ser}} \qquad (2)$$

Static power P_{leak} due to current leakage through nano devices in their OFF state,

$$P_{leak} = \frac{MV_{DD}^2}{2R_{OFF}/D} \qquad (3)$$

Dynamic power P_{dyn} due to recharging of nanowire capacitances.

$$P_{dyn} = \frac{C_{wire}V_{DD}^2}{4\tau} \qquad (4)$$

Where τ is the total circuit delay. The factors 1/2 reflect the

natural assumption that on average there is an equal number of CMOS inverters with Boolean 1 and 0. The dynamic power has an additional factor 1/2 describing the energy loss at capacitance recharging.

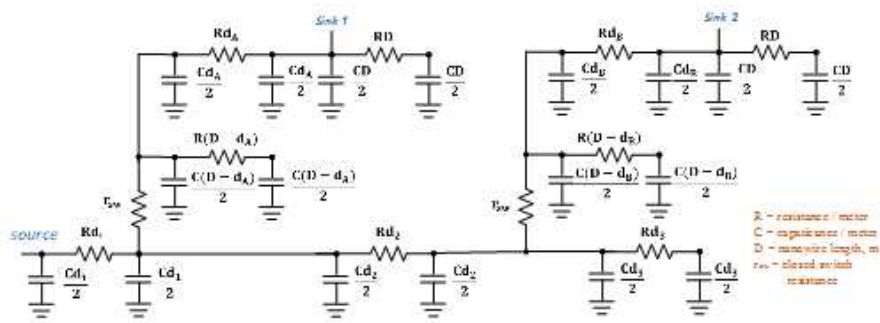Figure 5 shows the electrical model of nano wires and junctions of nano wires. According to Snider [13], (a) shows the electrically closed junction switches between the nanowire driven by the source and the two nanowires connected to the sinks. The electrical model (b) shows the physical coordinates of the nanowires and their closed junctions to derive nanowire resistance and capacitance.

Delay is estimated using the Elmore delay model; *Delay* (source → sink 1).

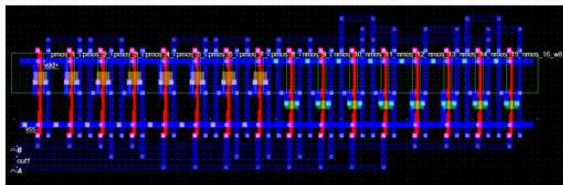$$\approx Rd1(4D + d1/2 + d2 + d3)C + 2rswDC + RdA(D + dA/2)C \tag{5}$$
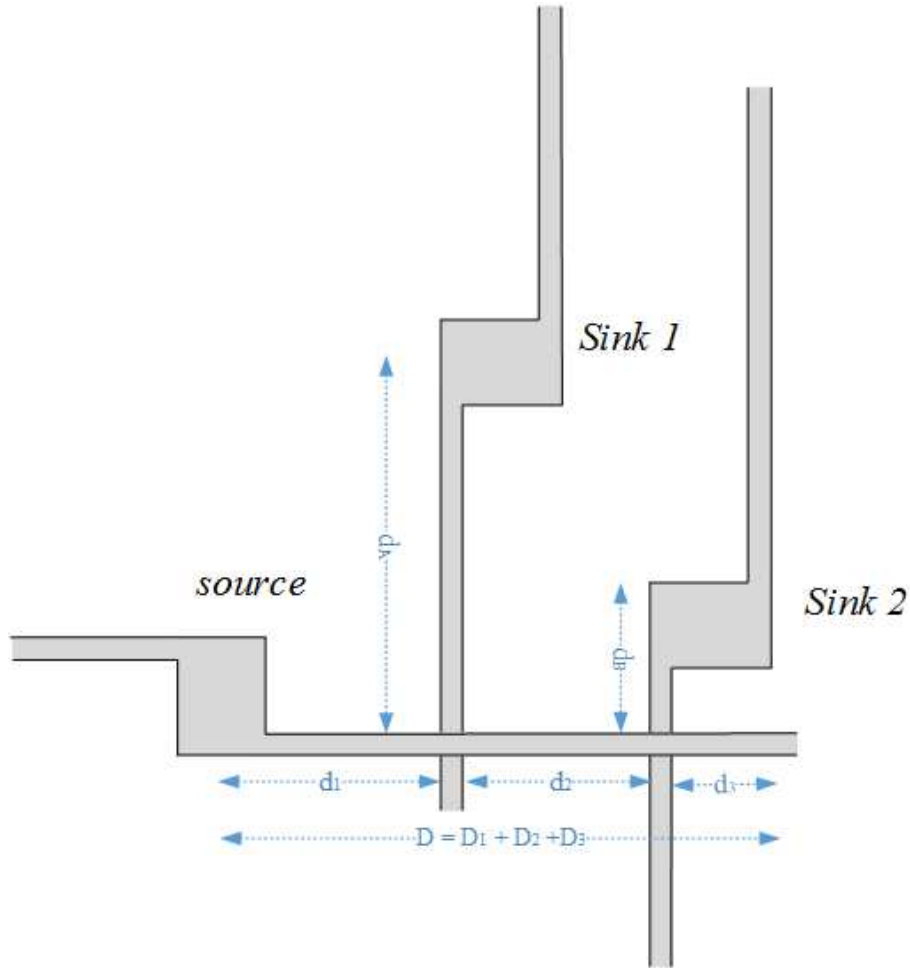
(a)

(b)

Figure 5. *Electrical model of nanowires and junctions. [13]*

4. Performance Testing

As discussed before, qNAND is special structure consisting of four Metal Oxide Semiconductor (MOS): two PMOS and two NMOS where four replica is used instead of only one element. Following figure 6 shows the layout of proposed qNAND. It's a two input one output NAND gate of quaded structure. Nand gate behaves as opposite to AND gate. In the following figure 6, there are two input A and B and corresponding output is shown. White color represents input A and green color represents input B and output is in red color. From the truth table of NAND gate we know that, if at least one input is low (0), output will be high (1). If both input is high (1) output is low (0). For example, in the time period of 0.6 ns, input A is low but input B is high resulting the output to be high. But in time period of 0.8 ns, both input A and B is high and the output is low. So, it is clear that, proposed qNAND gate is working correctly.
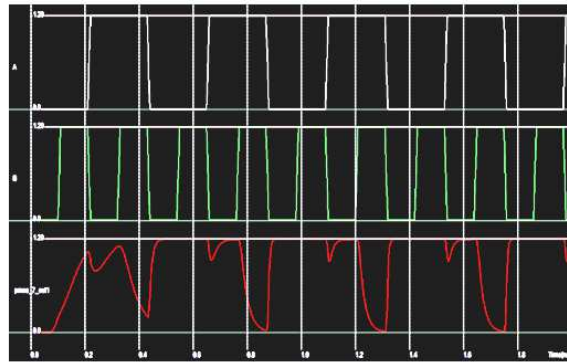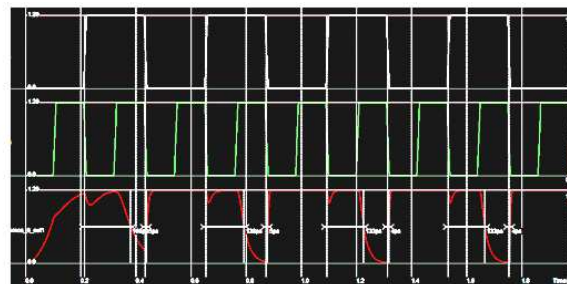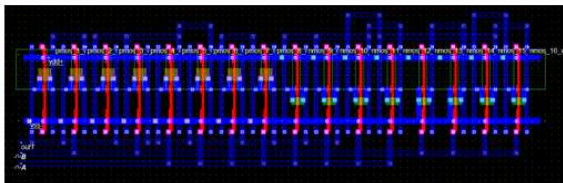

Figure 6. Proposed QNAND (a) layout and its (b) output.

*Figure 7. Proposed QNAND*open Series *(a) layout and its (b) output.*

For implementing fault tolerant voter circuit, we have used quaded structure NAND gate. To asses it's performance against different faults, proposed QNand is tested with various fault models such as stuck at 0, stuck at 1, bridging fault model.

4.1. Testing with Stuck at 0 Fault

Stuck at 0 is a basic fault model for testing performance of any design. In such cases, particular elements are set to be open. As a result the whole component fails to operate correctly. However, in the proposed qNAND, four transistor is used instead of one for increasing fault tolerance.

If the defects do not occur in any two parallel transistors, double stuck open or their corresponding bridge defects are tolerated. In the figure 7 (a), layout stuck at 0 fault is applied, transistor 1 and transistor 3 are set open thus stucking at a value of 0 all the time. As these two transistors are in series this fault is tolerable and correct output is given in figure 7(b).

On the other hand, double stuck open or their corresponding bridge defects are not tolerated if defects occurs in any two parallel transistors. In the figure 8 (a), transistor 1 and 2 are in parallel and opened thus stucking at 0 all time. As a result, circuit will fail to operate correctly. In the figure 8 (b), output of this fault injected QNand is shown.

4.2. Testing with Stuck at 1 Fault

Double–stuck short or their corresponding bridge defects are tolerated as long as they do not occur to any series transistors. This is shown in figure 9 (a) and figure 9 (b). Here, transistor 1 and 2 are shorted. As a result, both of the transistor are stuck at 1 throughout the period. But still now the QNand is providing correct output.

But if defects occurs in any two series transistors Double–stuck short or their corresponding bridge defects are not tolerated. This is shown in figure 10 (a) and figure 10 (b). Transistor 1 and transistor 3 are in series and they are shorted. Thus these transistors are stuck at 1 throughout the time period. So double stuck short and bridge defects are not tolerated in this case.

However, it may be concluded that, proposed Quaded Nand architechture (QNAND) is completely fault tolarable for

single defect cases. But for double defect cases, it is fault tolerable fulfilling some conditions.
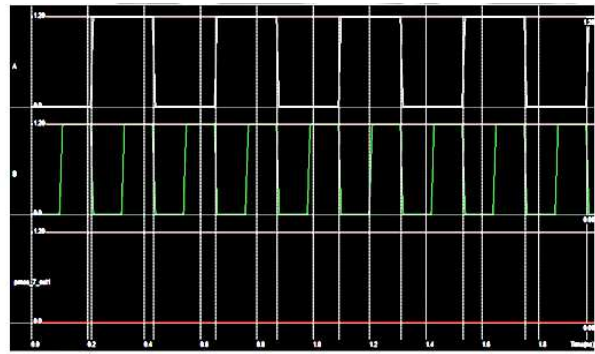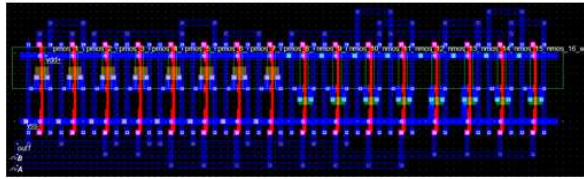

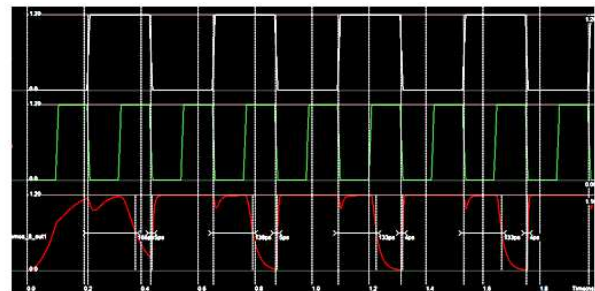***Figure 8.*** *Proposed QNAND parallel open (a) layout and its (b) output.*
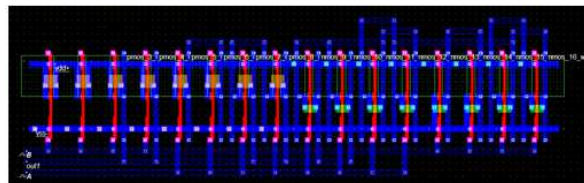

Figure 9. *Proposed QNAND Parallel short (a) layout and its (b) output.*
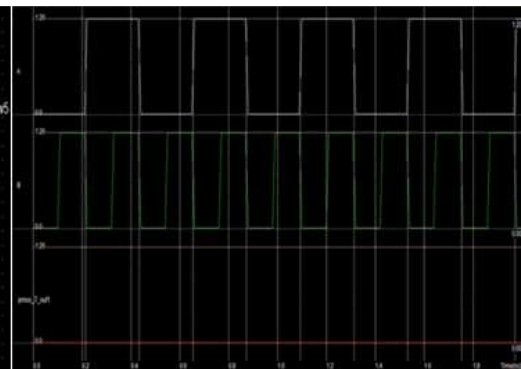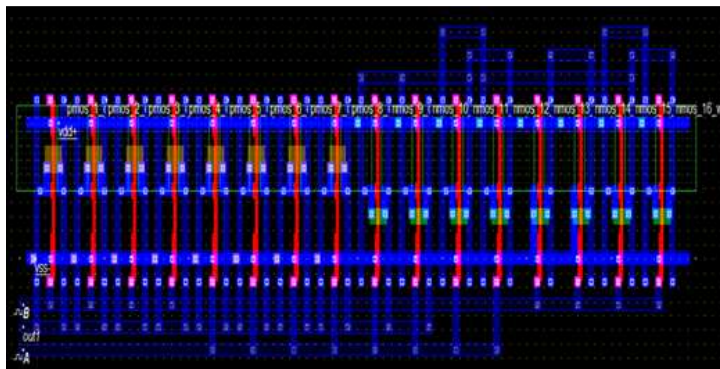

Figure 10. *Defects in Series (Double stuck short or their corresponding bridge defects) are not tolerated.*

5. Conclusion

In this work, the feasibility and effectiveness of quaded transistor structure has been investigated as a defect-tolerant technique at nano level. The proposed technique was found reliable against many permanent defects including stuck-open, stuck-short and bridging defects. Experimental results have demonstrated that the proposed technique provides significantly less circuit failure probability and higher reliability. The results have been investigated theoretically and by simulation.

Also, a suitable architecture has been proposed for NAND gate to be implemented in nano level. The CMOL based hybrid (NANO/CMOS) architecture is very much applicable for future electronics that has the capability to merge the existing CMOS level to future nano level.

References

[1] D. B. Strukov and K. K. Likharev. CMOL FPGA: A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices. Nanotechnology, 16: 888–900, 2005.

[2] Y. Huang, "Logic gates and computation from assembled nanowire building blocks," Science, 294: 1313–1317, 2001.

[3] Y. Chen, G.-Y. Jung, D. A. A. Ohlberg, X. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. Fraser Stoddart, and R. S. Williams, "Nanoscale molecular-switch crossbar circuits," Nanotechnology, 14: 462–468, Apr. 2003.

[4] D. Whang et al., "Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems," Nanoletters, vol. 3, no. 9, Sep. 2003, pp. 1255–1259.

[5]   H. Naeimi and A. De Hon, "A greedy algorithm for tolerating defective crosspoints in Nano PLA design," in Proc. Int. Conf. Field-Programmable Technol., 2004, pp. 49–56.

[6]   P. Samudrala, J. Ramos, and S. Katkoori, "Selective Triple Modular Redundancy (STMR) Based Single-Event Upset (SEU) Tolerant Synthesis for FPGAs," IEEE Transactions on Nuclear Science, Vol. 51, No. 5, pp. 2957–2969, Oct. 2004.

[7]   F. L. Kastensmidt, L. Sterpone, L. Carro, and M. S. Reorda, "On the optimal design of triple modular redundancy logic for SRAM-based FPGAs," Design, Automation and Test in Europe, pp. 1290–1295, Vol. 2, 2005.

[8]   T. Hogg and G. S. Snider, "Defect-Tolerant Adder Circuits With Nanoscale Crossbars," IEEE Trans. on Nanotechnology, vol. 5, no. 2, pp. 97–100, March 2006.

[9]   K. L. Jensen, "Field emitter arrays for plasma and microwave source applications," *Phys. Plasmas,* vol. 6, no. 5, pp. 2241-2253, 1999.

[10] K. K. Likharev and D. B. Strukov, "CMOL: Devices, circuits, and architectures," in *Introducing Molecular Electronics,* G. Cuniberti, G. Fagas, and K. Richter, Eds. Berlin: Springer, 2005, published as Chapter 16.

[11] Strukov D B and Likharev K K 2005 CMOL FPGA: "A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices," in *Nanotechnology* 16 888–900.

[12] Steinh¨ogl W, Schindler G, Steinlesberger G and Engelhardt M 2002 "Size effects in the electrical resistivity of polycrystalline nanowires", *Phys. Rev.* B 66 075414.

[13] Gregory S Snider, R Stanley Williams 2007, "Nano/CMOS architectures using a field-programmable nanowire interconnect", *Nanotechnology* 1835204.

[14] International Technology Roadmap for Semiconductors (ITRS) 2005 Available online at http://public.itrs.net/

[15] Veldhorst, M., et al. "Silicon CMOS architecture for a spin-based quantum computer." *Ar Xiv preprint ar Xiv: 1609.09700* (2016).

[16] Prinzie, Jeffrey, et al. "A single-event upset robust, 2.2 GHz to 3.2GHz, 345 fs jitter PLL with triple-modular redundant phase detector in 65 nm CMOS." *Solid-State Circuits Conference (A-SSCC), 2016 IEEE Asian*. IEEE, 2016.

[17] Kanvitha, P., and N. Naga Raju. "FAULT SECURE ENCODER ANDDECODER FOR NANO-MEMORY APPLICATIONS." (2016).

[18] Altun, Mustafa, Valentina Ciriani, and Mehdi Tahoori. "Computing with nano-crossbar arrays: Logic synthesis and fault tolerance." *2017 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2017.