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Electrical Performance and Stability of ZnO Thin-Film Transistors Incorporating Gadolinium Oxide High-k Dielectrics

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Abstract: This work investigates the performance and gate bias stress instability of ZnO-based thin film transistors (ZnO-TFTs) incorporating amorphous gadolinium oxide, a high-k dielectric material. ZnO thin films produced via radio frequency (RF) reactive magnetron sputtering were used as channel layers. The source/drain electrodes were achieved by the thermal evaporation of aluminium on a bottom gate inverted staggered ZnO TFT structure. Gadolinium oxide (Gd_2O_3) deposited by metal-organic chemical vapour deposition (MOCVD) served as the gate dielectric. The electrical characterisation of the ZnO-TFTs produced showed improvement in performance and stability in comparison to thermally-grown SiO_2-based ZnO TFTs fabricated under the same conditions. The effective channel mobility, on-off current ratio and subthreshold swing of the TFTs incorporating Gd_2O_3 dielectric were found to be 33.5 $cm^2 V^{-1}s^{-1}$, 10^7, and 2.4 V/dec respectively when produced. The electrical characterisation of the same devices produced with SiO_2 dielectrics exhibited effective mobility, on-off current ratio and subthreshold swing of 7.0 $cm^2 V^{-1}s^{-1}$, 10^6 and 1.4 V/dec respectively. It is worth noting that, the ZnO active layer was sputtered under room temperature with no intentional heating and post-deposition annealing treatment. On application of gate bias stressing on these thin film transistors, it was observed that threshold voltage instability increased with stress period in all device types. Transistors incorporating Gd_2O_3 however, were found to exhibit lesser threshold voltage related instability with regards to gate bias stressing in comparison to similar devices incorporating SiO_2 as gate dielectric. It was also observed that the effective mobility in both devices tend to stabilize with prolonged gate bias application. In this work, it is demonstrated that Gd_2O_3 dielectric is a potential alternative to SiO_2 for the fabrication of ZnO TFTs with improved performance and electrical stability under prolonged use.

Keywords: Zinc Oxide, Thin Film Transistors, Gd_2O_3, Performance, Gate Bias Stress Instability, High-K Dielectrics, Magnetron Sputtering, TFT

1. Introduction

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have so far been the main alternative to amorphous silicon (a-Si) TFTs for use in flat panel displays by industrialists, in applications where high speed switching is required such as in radio frequency applications. This has been mainly due to the relatively low electron mobility of amorphous silicon TFTs [1]. However, both the poly-Si and a-Si TFTs are non-transparent to visible light, thus would limit the aperture ratio of the active matrix arrays in flat panel displays and also suffer from light induced instabilities [2, 3]. Semiconducting metal oxides with large bandgap (thus, transparent to the visible region of the electromagnetic radiation, such as ZnO with a bandgap of ~3.37 eV), can be

used to fabricate high channel mobility TFTs (at temperatures significantly lower than those used in a-Si and poly-Si processes) and in addition offer a way to overcome light induced instability issues. Thin film transistors incorporating ZnO as active layer have been demonstrated to exhibit superior performance with different gate insulators [4-8]. These transistors have been found to exhibit high effective channel electron mobilities (μ_{eff}) that could lead to higher drive currents and faster device operating speeds (required for high frequency applications and as driver TFTs required for organic light-emitting diode displays).

Despite the performance (mobility) advantages offered by ZnO TFTs, threshold voltage instability as a result of a prolonged application of gate bias remains an issue [9-11]. This gate biased instability issue adds to another common form of instability reported in literature, resulting from ambient conditions after long time storage. Some authors have attributed such ambient related instability to adsorption of water vapour from the air as well as the depletion of oxygen vacancies [12, 13]. The purpose of this work is to demonstrate that gate bias related instability can be minimised by using a high-k gate dielectric such as Gd_2O_3 without degrading the device performance. This is motivated by the fact that the use of high-k dielectric enhances charge accumulation at the semiconductor/dielectric interface, thus enabling the TFTs to operate at lower gate voltages [14]. In addition, rare earth oxides including Gd_2O_3 have been reported to exhibit high-k dielectric properties with interface matching properties competing with those of the traditional SiO_2 [15] , currently considered the dielectric of choice in the microelectronics industry. High-k dielectrics present an opportunity to use thicker dielectric layers in TFT fabrication, resulting to reduced normal gate electric field strength at the semiconductor/dielectric interface. As a result of the low interface field, less electrical stressing is expected in such devices during prolonged operation. ZnO TFTs incorporating Al_2O_3 dielectric (another high-k material) have been found to exhibit improvements in both performance and gate bias induced instability [16, 17].

2. Experiments

In this work, ZnO TFTs were fabricated incorporating gadolinium oxide (Gd_2O_3), deposited by metal-organic chemical vapour deposition (MOCVD) [18], as a gate insulating layer. The source/drain (S/D) electrodes were formed by thermally-evaporating 100 nm thick aluminium (Al) patterned by shadow masks (defining the ZnO channel width/length ratio W/L=10:1). The ZnO channel layer thickness (40 nm) was obtained by a reactive radio frequency (RF) magnetron sputtering process using an oxygen/argon (O_2/Ar) flow rate (sccm) of 0.2/8, and an 8" diameter ZnO ceramic target of 99.999 % purity. The deposition was performed at room temperature with no intentional heating applying a moderate power of 15 W. The target to substrate distance was set at 6 cm. The ZnO layer was post-treated with O_2 (0.2 mTorr) for one hour immediately after deposition prior to breaking the vacuum in order to improve the film crystallinity and electrical stability in air [6, 19]. The finished TFT is a bottom-gate (n^+-silicon) inverted-staggered configuration as shown in figure 1.

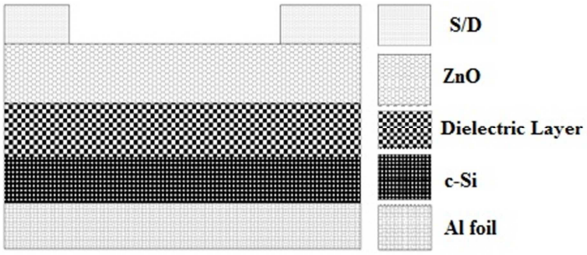

Figure 1. *Inverted staggered bottom-gate TFT structure.*

A similar TFT structure produced using thermally-grown silicon dioxide (SiO_2) as the gate insulator is also fabricated. For each set of devices, the ZnO layer was sputtered on the different dielectric layers (SiO_2 and Gd_2O_3) at the same time to reduce the possible effects of parameter variation during the deposition process. The film transmission data was obtained using a UNICAM UV/Vis spectrometer (UV 2). The surface morphology of films were characterised by atomic force microscopy (AFM) using a Park AFM XE-100 system, operating in the non-contact mode while electrical measurements (current-voltage (I-V) and capacitance-voltage (C-V)) characteristics were achieved by the HP4140B pico-ammeter and an HP4192A impedance analyser.

Prior to the TFTs fabrication, the dielectric layers (SiO_2 and Gd_2O_3) were electrically characterised using the metal-insulator-semiconductor (MIS) structure of figure 2. A (100) p-type silicon wafer with a resistivity of 1.25 Ω-cm with an ohmic aluminium (Al) back contact was used as substrate. The ohmic Al back contact was achieved by heat-treatment of evaporated Al on the p-Si for 30 minutes at temperature of 490°C in a carbolite gpc 12/65 furnace. The different dielectric films (Gd_2O_3 and SiO_2) were then deposited by MOCVD at a temperature of 400°C.

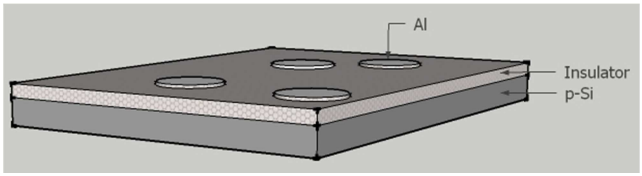

Figure 2. *MIS capacitor structure of Al/Gd_2O_3/p-Si.*

The MIS structure was completed by evaporating (100 nm thick) circular aluminium dots of 500 μm radii (0.0079 cm^2 area) using shadow masks onto the as-deposited Gd_2O_3 dielectric.

3. Results and Discussion

Figure 3 below shows the transmission data of a 150 nm-thick ZnO layer on glass (soda lime) using the same sputtering parameters and post-oxygen treatment as that used for ZnO TFT fabrication. An average transparency of over

85% over the visible region is observed with an absorption edge around 376 nm. The ZnO TFTs fabricated in this work uses a ZnO layer of only 40 nm thick, hence its transparency in the visible is expected to be quite close to 100%

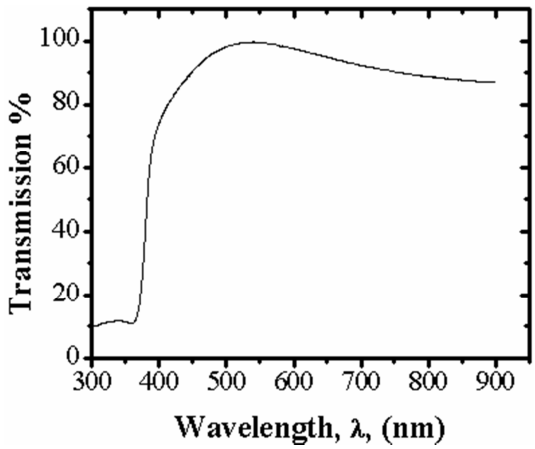

Figure 3. *Transmission data of a 150 nm thick sputtered ZnO on glass.*

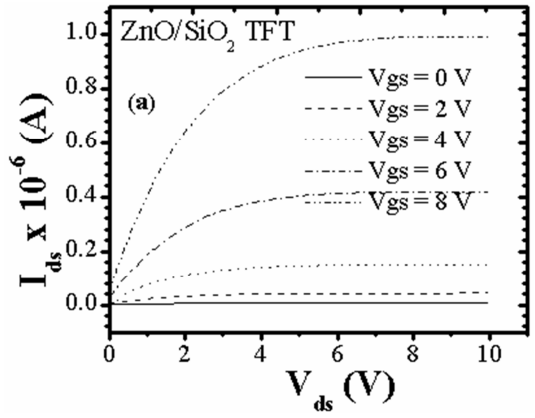

Figure 4. *Output characteristics (I_{ds}-V_{ds}) of ZnO-TFTs incorporating SiO_2 insulator.*

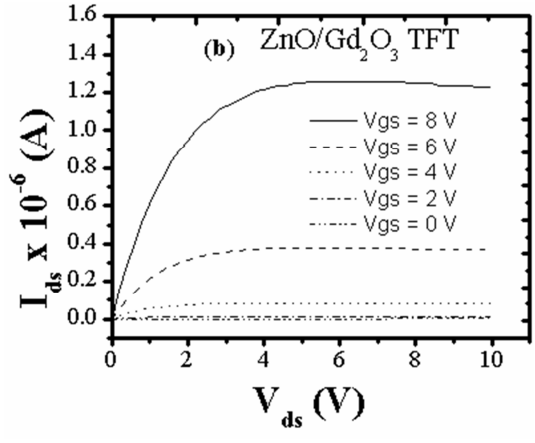

Figure 5. *Output characteristics (Ids-Vds) of ZnO-TFTs incorporating Gd_2O_3 insulator.*

The output characteristics of the two sets of as-fabricated TFTs incorporating different dielectrics are shown in figures 4 and 5. In both output characteristics, saturation is clearly observed, an indication of similarities in film doping concentrations (depletion width). The absence of drain current off-set at a drain-to-source voltage, V_{ds}= 0 V in figures 4 and 5 suggests that both transistors exhibit Ohmic behaviour at the Al/ZnO contacts.

Figures 6 and 7 are the atomic force microscopy images showing the surface morphology of ZnO layers deposited on Gd_2O_3 and SiO_2 respectively under the same condition as those used for the TFTs fabrication. The morphology of the two surfaces appears similar in terms of grain size and shapes. The surface rms roughness of the ZnO film is 0.7 and 0.9 nm on Gd_2O_3 and SiO_2 substrates respectively. Despite the fact that the ZnO material was deposited under identical sputtering conditions to the same thickness, the resulting surfaces appear to be moderately different. The corollary of which suggests that the ZnO/insulator interfaces are also likely to be different in terms of potential charge trapping sites, which may affect the TFT performance.

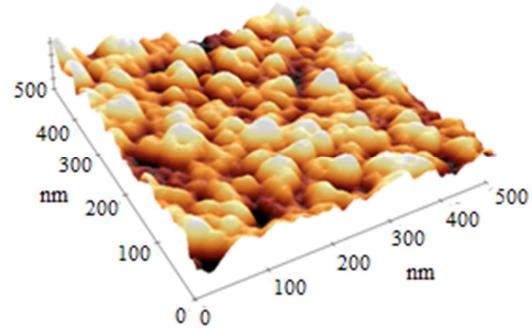

Figure 6. *Morphology of sputtered ZnO layer on gadolinium oxide insulator as determined by atomic force microscopy.*

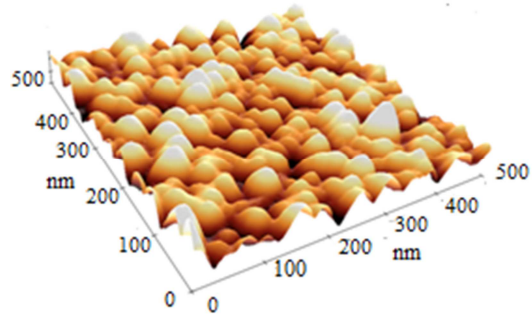

Figure 7. *Morphology of sputtered ZnO layer on silicon dioxide insulator as determined by atomic force microscopy.*

Electrical characterization of the Gd_2O_3 and SiO2 films were carried out using a combination of I-V and C-V characterisation techniques. C-V measurements were recorded by sweeping a direct current (DC) bias superimposed on an alternating current (AC) signal of 1 MHz (and at 25 mV) from inversion to accumulation and back to inversion. Prior to any C-V measurements, the leakage current through the MIS structures was first measured. In this regard, typical leakage currents were found to be of the order of 10^{-11} A for both films; however, the leakage current is thickness dependent (the thicknesses of the SiO_2 and Gd_2O_3 films used in this work were 100 and 82 nm, respectively).

Figures 8 and 9 show a typical C-V characteristics at two different frequencies for Gd_2O_3 SiO_2 films respectively.

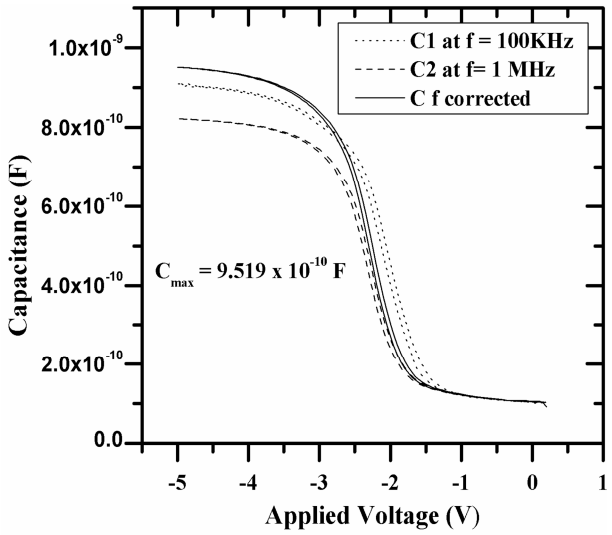

Figure 8. *Typical C-V characteristics of a Gd_2O_3 MOS structure together with the frequency correction performed at measurement frequencies of 100 KHz and 1 MHz.*

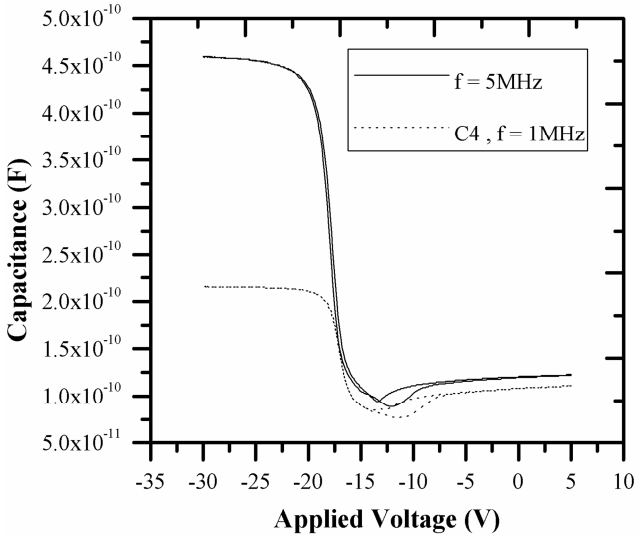

Figure 9. *Typical C-V characteristics of a SiO_2 MOS structure at measurement frequencies of 1MHz and 5MHz.*

It is evident that there is some variation in the capacitance of the materials with the AC signal, where the maximum capacitance increases with an increase in frequency. The true Capacitance C was extracted from two different capacitance values C_1' and C_2' measured at frequencies of $f_1 = 100\ KHz$ and $f_2 = 1\ MHz$ respectively using equation (1) as proposed by Yang and Hu [20] for case of Gd_2O_3 dielectric. From the C-V curves in figures 8 and 9, only negligible hysteresis is observed following a voltage sweep from accumulation to depletion and back. An indication of low trapping centres.

$$C = \frac{f_1^2 C_1'(1+D_1') - f_2^2 C_2'(1+D_2')}{f_1^2 - f_2^2} \quad (1)$$

Where D_1' and D_2' $_k$ are the dissipations measured at the frequencies f_1 and f_2 respectively.

A comparison of the transfer characteristics of 100 µm channel length ZnO TFTs (figure 10) fabricated on the different dielectrics suggests that ZnO TFTs incorporating Gd_2O_3 gate insulators have superior induced charge (Q_{ind}) in comparison to SiO_2-based TFTs.

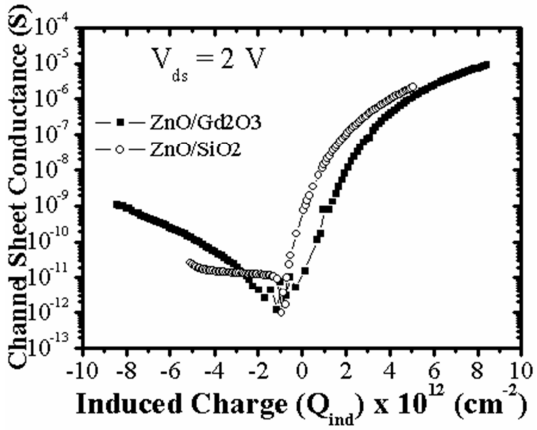

Figure 10. *A typical normalized gate transfer characteristics for ZnO TFTs incorporating Gd_2O_3 (solid squares) and SiO2 (opened circles).*

The data in figure 10 shows a plot of the normalised channel sheet conductance G $(\Omega cm)^{-1}$, versus total induced charge density Q_{ind} (electrons/cm^2) at the interface. This normalisation ensures that the performance parameters are measured under identical electric fields to account for the difference in equivalent oxide thickness for the different insulator layers. The induced charge density Q_{ind} is calculated from the gate voltage V_{gs} while G is calculated using the output current I_{ds} (equations (2) and (3)).

$$G = \frac{I_{ds}}{V_{ds}(W/L)} \quad (2)$$

$$Q_{ind} = \left(\frac{C_{ins} V_{gs}}{q}\right) \quad (3)$$

Where V_{gs} is the gate bias, C_{ins} the gate insulator layer capacitance, I_{ds} is the source drain current and W/L is the width/length ratio of the ZnO active channel. The properties of the films used are summarised on table 1.

Table 1. *Film properties (SiO_2 and Gd_2O_3).*

Film	Thickness (nm)	Dielectric Constant	Refractive Index
SiO_2	100	3.30	1.457
Gd_2O_3	82	9.87	1.852

Both the SiO_2 and Gd_2O_3 devices demonstrate a negative turn-on voltage (V_{On}) of -5.3 and -4.7 V with corresponding threshold voltages (V_T) of 23 V and 20 V respectively. The negative turn-on voltage can be attributed to a higher background concentration of n-type carriers in the semiconductor layer of the Gd_2O_3 devices, which would also have a direct effect on V_T. The On-Off current ($I_{On\text{-}Off}$), measured as the ratio of the maximum to minimum I_{ds}, is approximately 10^6 and 10^7 for the SiO_2 and Gd_2O_3 transistors respectively. More significantly, the Off-state leakage current

is more than two orders of magnitude higher in ZnO/Gd_2O_3 TFTs. The subthreshold slope (S) for the SiO_2 devices is 1.4 V/dec, lower than that observed in Gd_2O_3-based TFTs (typically ~ 2.4 V/dec), the subthreshold slope is indicative of the density of the interface states (N_{ss}) [21], and the maximum density of states (N_{ss}^{max}) present at the interface between ZnO and the gate dielectric is estimated by the relation in equation (4).

$$N_{ss}^{max} = \left[\frac{S.\log(e)}{kT/q} - 1\right]\frac{C_{ins}}{q} \quad (4)$$

Where k is the Boltzmann's constant, T is the measurement temperature, q the elemental electron charge, S the subthreshold slope, and C_{ins} the capacitance of the dielectric layer. In this work, N_{ss}^{max} values of $1.1 \times 10^{13}\ cm^{-2}$ and $2.4 \times 10^{12}\ cm^{-2}$ were obtained for ZnO on Gd_2O_3 and SiO_2 respectively. This suggests that the interface of the ZnO material with SiO_2 is likely to have less dangling bonds and potential sites for charge trapping than that made with Gd_2O_3. Of particular importance in terms of potential device application, the effective channel mobility extracted from the linear region of the transistor transfer characteristics at a drain bias of 2 V is 33.5 $cm^2V^{-1}s^{-1}$ for the ZnO/Gd_2O_3 TFT and 7.0 $cm^2V^{-1}s^{-1}$ for the ZnO/SiO_2 TFT. Given the details above concerning rms roughness and density of trap states at the interface, the mobility values seem counterintuitive. However, despite the fact that the value of N_{ss}^{max} for the Gd_2O_3 devices are almost an order of magnitude higher than observed in SiO_2 devices, the disparity in mobility value suggests that the nature of the trap states are different in the two material systems. Using these results, one could therefore speculate that the interface of the Gd_2O_3 devices may have a higher concentration of fast states which have short trapping times and hence do not affect the carrier mobility to any great extent. Furthermore, this effect may as well be compensated by the greater induced charge at the interface of ZnO/Gd_2O_3 as observed above.

The ZnO material utilised in this work was deposited at room temperature and received no post-deposition heat treatment; and the impressive value of channel mobility in combination with the Gd_2O_3 grown from new Gadolinium precursors [18], highlights its potential for TFT applications. However, further work is necessary to determine definitively the effects of the different insulators on the interface with the ZnO and, by extension, the manifestation of those effects in device performance.

A study of gate bias stress instability of the two sets of TFTs was also undertaken to investigate further the effects of the different insulating materials on prolonged gate application. In order to compare the electrical stabilities across TFTs incorporating dielectric layers with different thicknesses and dielectric constants; a stress bias (V_{SiO_2}) of 10 V was set for SiO_2-based TFTs producing an interface field of 1 MV/cm at the ZnO/SiO_2 interface. An equivalent stress bias (V_B) for the high-k dielectric (Gd_2O_3) was defined from this as the gate bias that will induce the same amount of charge (Q_{ind}) at the ZnO/Gd_2O_3 interface, and was calculated to be 8.2 V using equation (5) below.

$$V_B = \frac{C_{SiO_2}V_{SiO_2}}{C_{high-k}} \quad (5)$$

Where C_{SiO_2} and C_{high-k} are the capacitances of the SiO_2 and Gd_2O_3 dielectric layers respectively. The implication of this is that during gate bias stressing, the same quantity of charges accumulate at the semiconductor/insulator interface.

On application of a gate bias stress, it was observed that positive gate bias stress shifted the entire I-V characteristics to the right while a negative gate bias stress resulted to a shift to the left. A typical behaviour of the ZnO TFT incorporating SiO_2 upon gate bias stress is shown in figures 11 and 12 below.

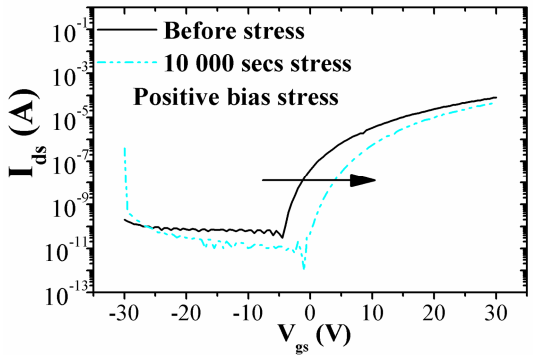

Figure 11. *Typical instability in SiO2 based ZnO TFT as a result of gate bias stress showing the shift in the transfer characteristics to the right following positive gate bias stress.*

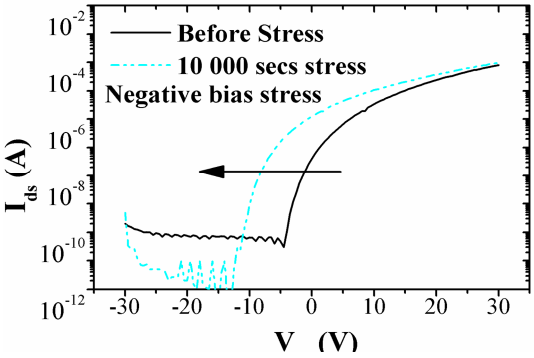

Figure 12. *Typical instability in SiO2 based ZnO TFT as a result of bias stress showing the shift in the transfer characteristics to the left following a negative gate bias stress.*

Upon release of the gate stress condition, the transfer characteristics of both TFT device types returned to within 1 V of their initial positions after a rest time of three days.

The shifts in transfer characteristics directly gave rise to variations in both the threshold and turn-on voltages as displayed by the results in figures 13 and 14.

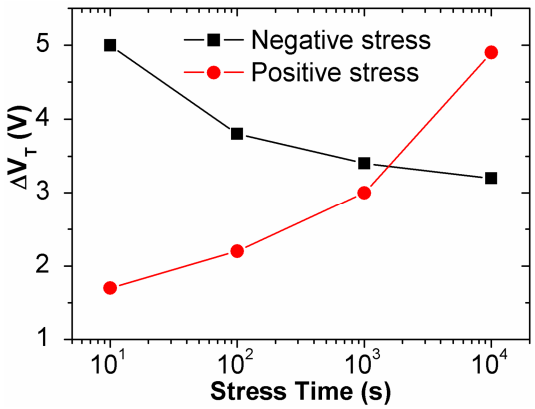

Figure 13. *Typical instability in SiO_2 based ZnO TFT showing variation in threshold voltage following positive and negative bias stresses.*

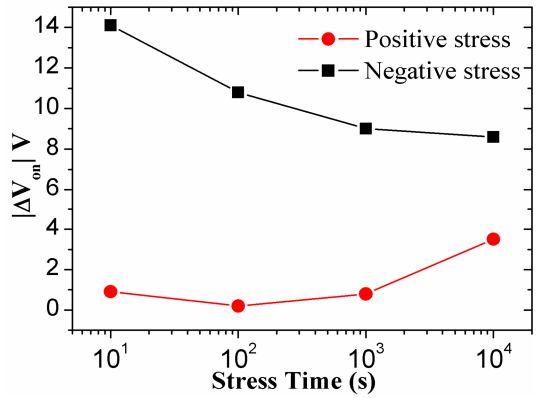

Figure 14. *Typical instability in SiO_2 based ZnO TFT showing variation in turn-on voltage following positive and negative bias stresses.*

The results reveal that TFTs incorporating Gd_2O_3 only exhibited an initial variation in the effective mobility (< 5 $cm^2V^{-1}s^{-1}$ after a stress time of 10 s) but remained fairly stable for stress times up to 10^4 s (figure 15), while SiO_2-based devices show continuous variation in effective mobility throughout the entire stress period. This constancy in effective mobility after prolonged gate bias stressing suggests that charge trapping sites involve are very close in energy.

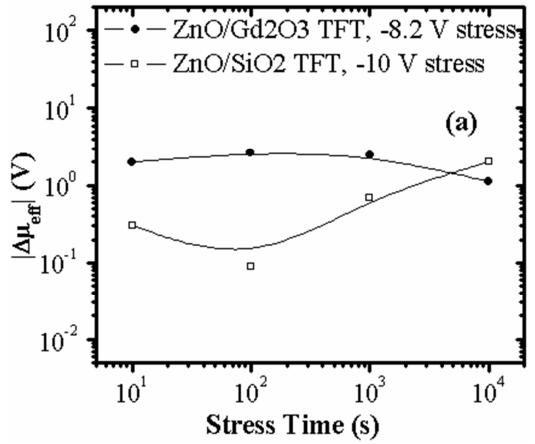

Figure 15. *Variation of effective mobility with stress time for ZnO-TFTs incorporating SiO_2 and Gd_2O_3. The stress is performed at voltages that give rise to identical interface fields.*

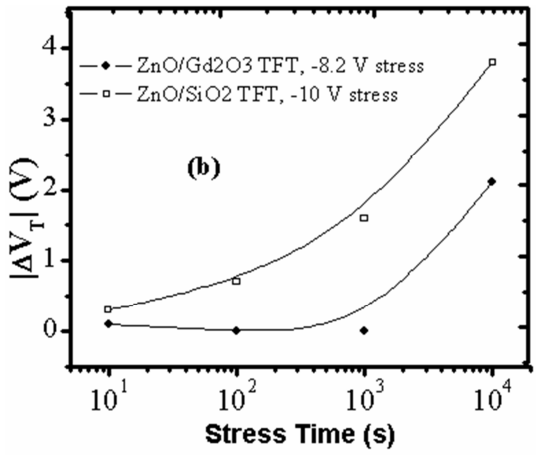

Figure 16. *Variation of threshold voltage with stress time for ZnO-TFTs incorporating SiO_2 and Gd_2O_3. The stress is performed at voltages that give rise to identical interface fields.*

In addition, the improved stability exhibited by Gd_2O_3-based ZnO TFTs is confirmed by the weak variation of V_T following gate bias stressing relative to their SiO_2-based counterparts (figure 16). In fact for these devices, V_T remains fairly constant for upto a gate bias stress time of 10^3s. Again, the improved relative stability of the Gd_2O_3 devices when compared to the SiO_2-based TFTs demonstrates the integration of high-k dielectric materials (Gd_2O_3) in ZnO TFT fabrication.

4. Conclusion

In this work, the effects of prolonged gate bias stress on ZnO TFTs using MOCVD deposited Gd_2O_3 as gate dielectric is reported. A comparative study of the electrical properties of ZnO-TFT devices fabricated with SiO_2 and Gd_2O_3 revealed that the latter exhibits superior performance with respect to effective mobility. The improved performance of the ZnO/Gd_2O_3 TFT is attributed to the higher dielectric constant of the Gd_2O_3 which results to an increased capacitance. Since high-k dielectric materials have greater capacitance, the TFT channel requires a lower gate voltage to form an equivalent accumulation layer at the ZnO/insulator interface. Thus, devices can operate at a much lower gate voltage. Furthermore the use of thicker high-k dielectrics to achieve a large capacitance is also expected to reduce the influence of the gate electric field at the semiconductor/dielectric interface. All of these are likely to reduce the effect of bias stressing on the operation of the TFT. Furthermore, it has been demonstrated that a combination of the Gd_2O_3 material coupled with the room-temperature deposited ZnO layer used in this work, do not only support the potential benefits of incorporating high-k materials in ZnO TFTs, but also demonstrates high channel mobility and enhanced device stability in devices incorporating high-k dielectrics. Both of these factors may help to address both the performance and gate bias-stress related issues in ZnO TFTs [22].

Acknowledgements

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