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A performance comparison of CMOS voltage-controlled ring oscillators for its application to generation and distribution clock networks

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Abstract: In this work, a performance comparison of expanded CMOS voltage-controlled ring oscillators for non-resonant local clock generation and distribution networks is presented. Several differential and single-ended ring oscillators are designed and fabricated using long interconnection lines to achieve wide coverage chip. A test chip containing the several oscillators was fabricated using an Austria Microsystems (AMS) 0.35 μm CMOS technology. Experimental results show that it is possible to generate and distribute high frequency signals (GHz range) on a relativity large area (coverage) and low phase noise using non-resonant ring oscillators. This represents an attractive alternative for the design and implementation of local Clock Generation and Distribution Networks for systems on chip.

Keywords: Ring Oscillators, VCOs, Clock Networks, CMOS VLSI

1. Introduction

Nowadays, design of high- performance processors that perform many functions at high speed and low power consumption is of vital importance for the implementation of multimedia equipment (e.g. computers, cell phones, video games, video cameras, audio players, etc.). In high-performance microprocessors, a large number of functions are carried out in a synchronous digital way; therefore, the incorporation of a timing system responsible for generating and distributing the synchronization signals is indispensable.

In a timing system, commonly used in current microprocessors, the clock signal is generated in a single point using a Phase Locked Loop (PLL) circuit and globally distributed to all points (loads) or sinks where it is needed using a global clock distribution network (such as H-tree, mesh, or others) implemented by buffers and interconnection lines as shown in Fig. 1. The Global Clock Network (GCN) is widely used in the synchronization of integrated systems [1, 2]; however, their use is reaching its limit. The main problem associated with global networks is that the operation frequency is inversely proportional to the coverage area, i.e. a signal generated at a higher operation frequency can be distributed over a shorter distance (see Fig. 1), i.e. smaller Integrated Circuits (ICs). This is a consequence of the physical limitations of the long and global interconnection lines, which currently determine the minimum delay and impose a maximum distribution distance [3].

Today, in order to solve some problems associated with the GCN, some of the design philosophies that are under study are networks using distributed oscillators [4-11], and cooperative or connected ring oscillators [12-18]. In this work, we make use of the last philosophy and the networks are named Local Clock Generation and Distribution Networks (LCGDN) [4, 6]. In a LCGDN (Fig. 2) the clock signal is simultaneously generated and distributed at different points throughout the integrated circuit or chip; thus, the coverage area is reduced which allows to generate and distribute signals at higher operation frequencies and low time uncertainty (low skew and jitter) compared with using the GCN philosophy.

Interconnecting and coupling a set of ring oscillators can implement a LCGDN. In general, there are two design approaches of local networks, which are classified according to the type of oscillator used in their implementation. The first one is the *resonant local network* using resonant oscillators (standing waves, rotary waves and LC oscillators) based mainly on transmission lines [14,

15, 20]. The second one is the *non-resonant local networks* based on the interconnection and coupling of ring oscillators based on gain-delay stages [6, 13, 19]. Here we deal with the second approach: *Non-resonant* local networks based on expanded differential delay-stage ring oscillators. The paper is organized as follows: Section 2 shows general considerations for ring oscillators. The voltage-controlled ring oscillators topologies for local clock generation and distribution networks analyzed are presented in Section 3. In the section 4, the expanded single-ended and differential ring oscillators for LCGDN are simulated. Moreover, experimental results and analysis of the several ring oscillators fabricated are carried-out. Finally, Section V shows the conclusions of this work.

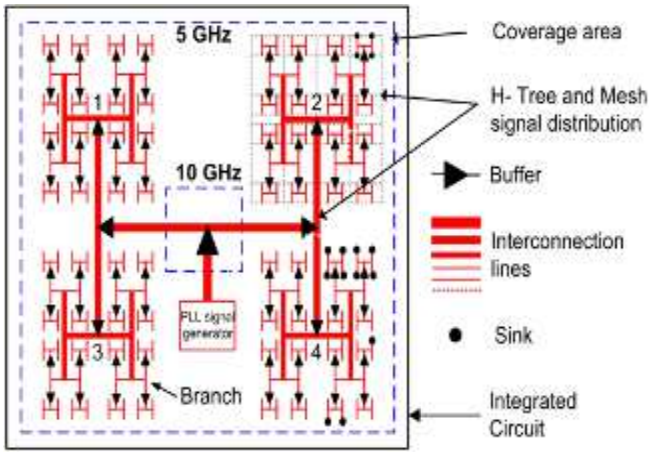


Figure 1. *Global Clock Generation and Distribution Network*

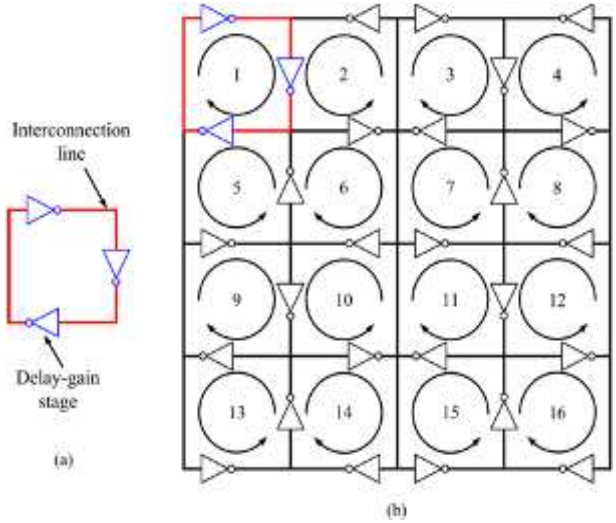


Figure 2. *Local Clock Generation and Distribution Network: (a) basic cell, (b) A LCGDN implemented by sixteen coupled and interconnected ring oscillators.*

2. Basic Principles of Ring Oscillators

Clock signals are the heartbeats of synchronous systems, and the simplest technique for on-chip generation of a clock signal is to use a basic ring oscillator, as shown in Fig. 2. The implementation of the local clock no-resonant network is realized by repeating the basic oscillator that generates the clock signal in conjunction with the use of interconnection lines that connect the oscillators and distribute the signal generated by the basic oscillators. In this way, the design of the whole network is reduced to the design and optimization of the basic oscillator.

A CMOS ring oscillator is a feedback circuit composed entirely of active devices that generates by itself a periodic signal at frequency ω_o. It is implemented by *N*-gain stages in a close loop, and generates a periodic signal, if and only if, the Barkhausen´s criteria are satisfied [20]:

$$|H(j\omega_o)| \geq 1 \tag{1}$$

$$\angle H(j\omega_o) = 180^o \tag{2}$$

where $|H|$ is the loop gain, and $\angle H$ is the phase shift around the loop. $\omega_0=2\pi f$

The operation frequency in a ring oscillator is given by:

$$f = \frac{1}{2N(t_d + t_l)} \tag{3}$$

where N and t_d are the number and delay of the gain stages (named delay-stages) and t_l is the delay associated with the interconnection lines. In a non-expanded oscillator $t_l \ll t_d$ and $f \approx 1/2Nt_d$.

As can be seen from above equations, the operation frequency is inversely proportional to the number and propagation delay time of the gain stages. Therefore, reducing the number of gain stages, and/or reducing the propagation delay time of the gain stages can increase the frequency in a basic ring oscillator. The first is the most interesting option because by reducing N besides increasing the frequency, the area, power consumption and the noise are also reduced.

According to published results, the operation frequency, power consumption, and noise of a ring oscillator can be substantially improved by using only a single gain stage [22, 23]. However, by using only one gain stage it is more difficult to satisfy the Barkhausen oscillation criteria given by equations (1) and (2). Nowadays, with the continuous down scaling of the fabrication CMOS technologies, the operation frequency, the power consumption, and noise of a ring oscillator can be substantially improved even using a large number of gain stages. In published papers about of voltage-controlled ring oscillators, several topologies implementing up to 9 gain stages have been proposed [21-28, 33, 35, 37, 43]. The use of a larger number of gain stages in a ring oscillator, allows the satisfaction in an easier way the Barkhausen oscillation criteria; nonetheless, the main disadvantage is that the operation frequency is reduced in accordance with equation (3). In order to overcome this frequency limitation, one of the philosophies widely used is the design of ring oscillators with multiple feedback loops [23].

3. Voltage-Controlled Ring Oscillators for Local Clock Generation and Distribution Networks

There have been reported many single-ended and differential ring voltage-controlled oscillators, with the generic topologies shown in Fig. 3. In this work, the emphasis on differential configurations is made because they have multiple advantages [25]. The single-ended (three delay-stages) topology is considered just for comparison purposes.

After a first qualitative revision of papers about of ring Voltage-Controlled Oscillators (VCOs) reported at the open literature and implemented in a standard CMOS process, eight VCOs implementations were selected for being quantitatively analyzed. These VCOs exhibit good characteristics such as high operation frequency, reduced number of delay-stages and reduced power consumption. The eight VCOs considered are shown in the figures 4 to 11 [21-28]. Each oscillator was designed using electrical parameters from an Austria Microsystems 0.35um CMOS technology. In order to verify its performance, the oscillators were tested using a static differential flip-flop and a single-ended dynamic flip-flop (Fig. 12).

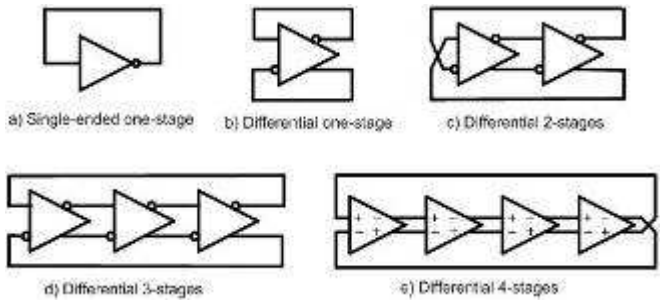


Figure 3. *Voltage-controlled ring oscillator topologies*

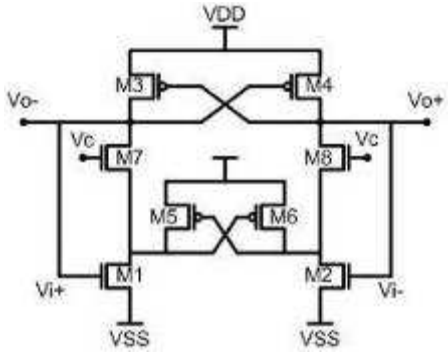


Figure 4. *One-stage D-latch VCO from Ahmed [22]*

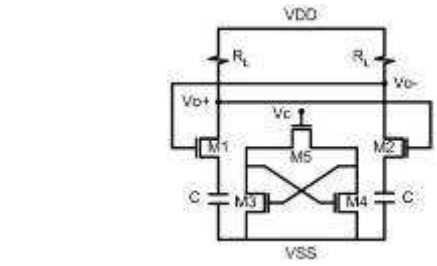


Figure 5. *One-stage VCO from Mostafa [21]*

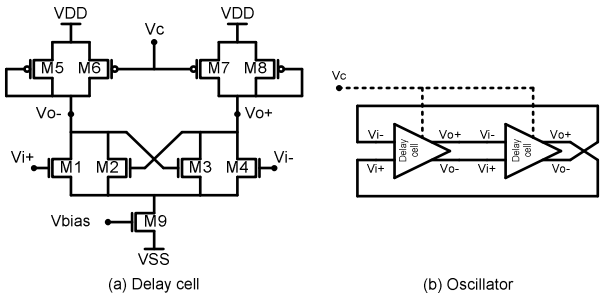


Figure 6. *Two-stages VCO from Daniel [24]*

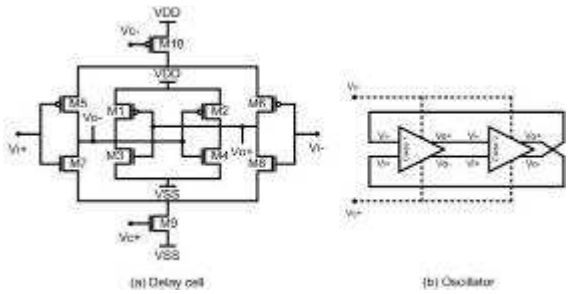


Figure 7. *Two-stages VCO from Liang [25]*

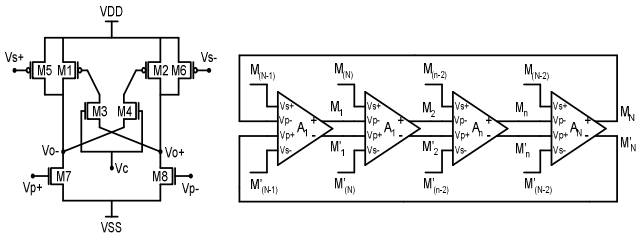


Figure 8. *Four-stages VCO from Yalcin [23]*

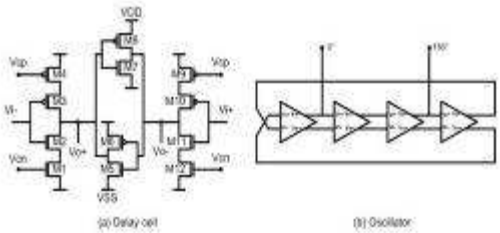


Figure 9. *Four-stages VCO from Joeres [26]*

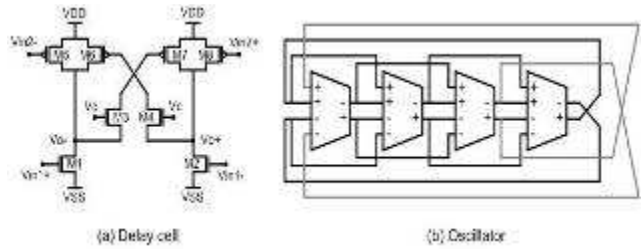


Figure 10. *Four-stage differential VCO using dual-delay path technique From Park [27]*

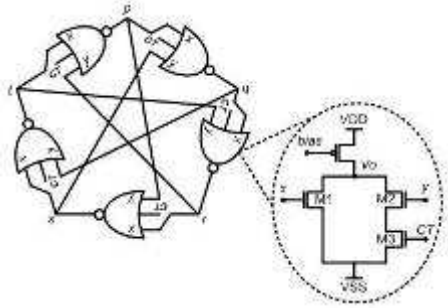


Figure 11. *Five-stages VCO using interpolation technique from Fadi [28]*

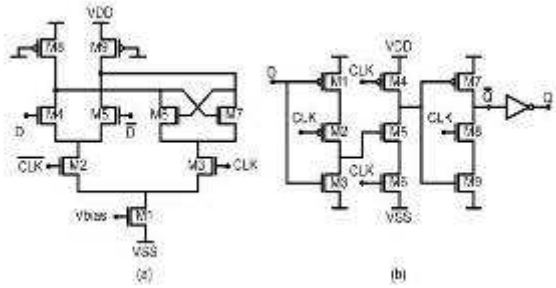


Figure 12. *Loads: a) Static differential Flip-flop, b) Dynamic Single-ended Flip-flop*

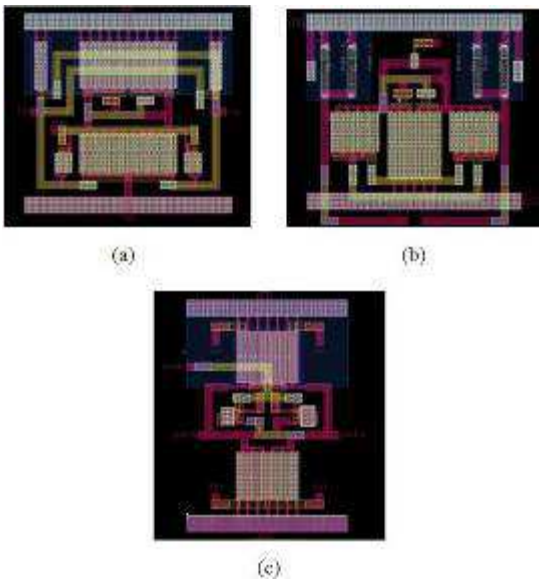


Figure 13. *Layouts of the high-performance VCOs: (a) Ahmed, (b) Mostafa, (c) Yalcin*

In figure 13 the layout of three high-performance oscillators are shown. The H-spice simulation results are presented in the Table I. Figures 14 and 15 show the transfer function and the waveforms output of the several designed VCOS, respectively.

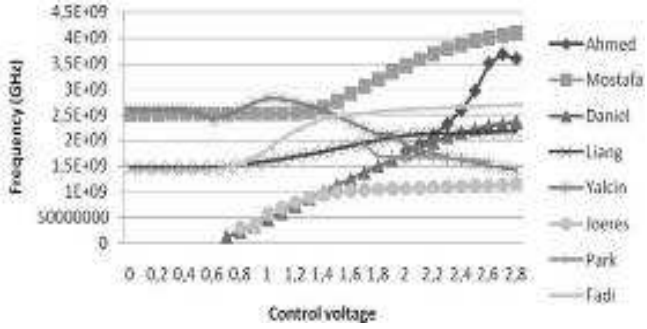


Figure 14. *Transfer functions of the ring oscillators*

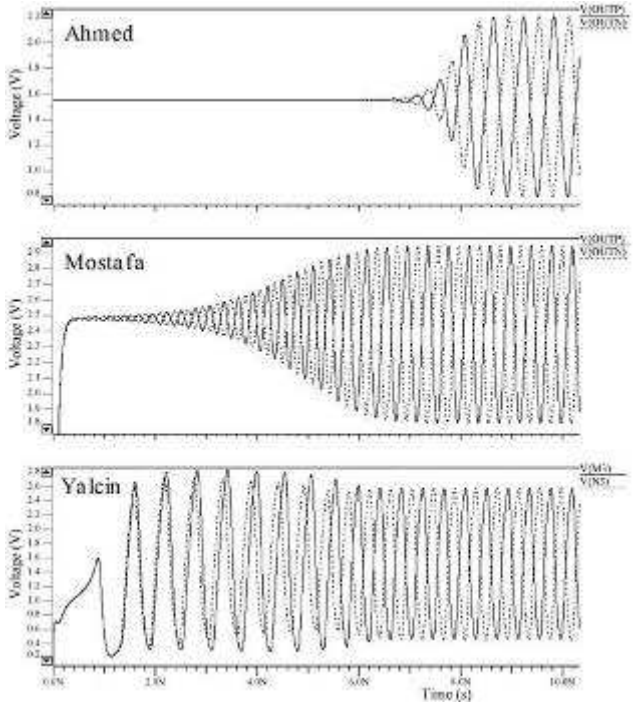


Figure 15. *Waveforms of the high-performance VCOs*

From Table 1 and figure 14 we can see that the highest frequencies are obtained for the VCO`s of one-delay stage; however, its amplitude is reduced compared with that of the others. The Yalcin`s oscillator even though it is constituted by four stages, it is the best VCO from the point of view of power consumption, since only it consumes 25% compared with Ahmed, and 37.3 % with respect to that of Mostafa. The VCO with highest wide tuning range is of the Daniel (1.81 GHz). Considering the wave form of the signal, the Yalcin`s oscillator produces a wave of major quadrature due to the biggest sweep of voltage (up to 3 volts in accordance with the table 1). We can see that in spite of the differences, the VCOs of Yalcin and of Mostafa demostrate the best performance. Finally, we concluded from these results, that not necessarily the VCO`s with a minimum number of stages are those that result with a better performance.

4. Expanded Voltage-Controlled Ring Oscillators for LCGDN

In section 3, the ring oscillators were designed in a conventional way, i.e. using short interconnection length between delay-gain stages of the ring oscillator. In this section, in order to analyze the performance of the single–ended and differential oscillators for the LCGDN, the design of expanded oscillators that simultaneously generate and distribute (in combination with long interconnection lines) high frequency signals over a given area is presented.

4.1. Single-ended Three-delay stage oscillators.

Several single-ended ring oscillators using interconnection lines with *w=2* µm and lengths *l=70, 1000,1500, 2000,* and *3000µm* were designed and fabricated using the Austria Microsystems 0.35 um process, a power supply of 3.3 V, and the Metal 4 level for the interconnection lines. Figure 16 shows the scheme of an expanded three-stage single-ended ring oscillator.

Table 1. *Hspice simulation results of the oscillators (V_{DD} = 3.3V)*

Parameter	Ahmed	Mostafa	Daniel	Liang	Yalcin	Joeres	Park	Fadi
Delay-stages (*N*)	1	1	2	2	3	4	4	5
Frequency (GHz)	1.8-3.2	2.2-3.7	0.19-2	1.3-1.9	2.6-1.4	0-0.96	0.94-0.8	1.2-2.4
Tuning range (GHz)	1.4	1.5	1.81	0.6	1.2	0.96	0.14	1.2
Power (mW)	7.5-8.5	13.4-12	1 - 14	9.2-12.6	2-3	0 - 5	12 - 13	6.8 – 8
Output voltage (V)	1.1-0.3	1.5-0.75	0.7-0.75	2.3-1.9	2.3	2.1-2.6	3.17 - 3	2.3-1.4

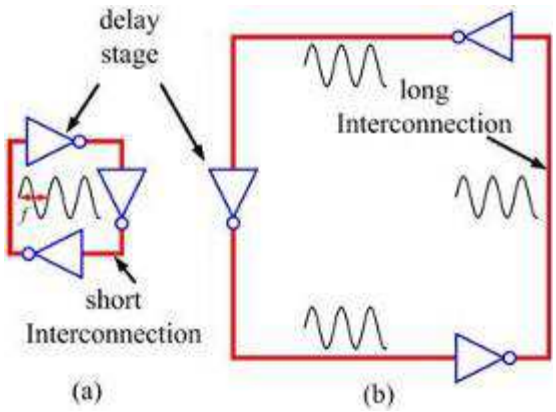


Figure 16. *Ring oscillator (a) Non-expanded, (b) Expanded*

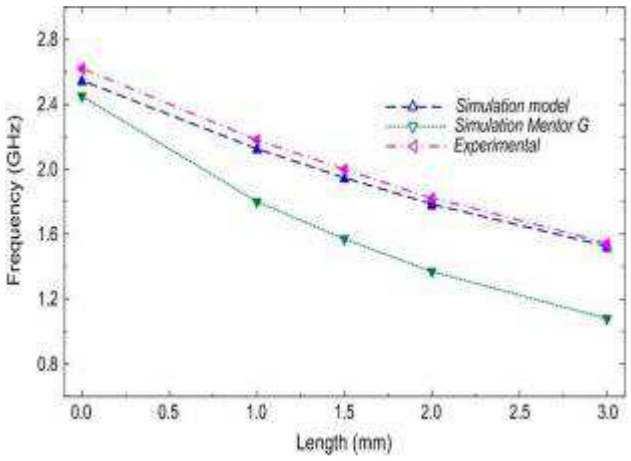


Figure 17. *Experimental and simulated operating frequency of single-ended three-stage ring oscillators.*

In figure 17 the experimental and simulated operating frequency performance for the implemented three-stage expanded ring oscillators varying the length of the interconnection lines is shown. In this figure, the corresponding simulated data are obtained considering the parasitic effects associated with the delay stages while the interconnection lines are represented by the equivalent circuit model as is given in [29].

Figure 18. *Experimental transient response of the fabricated single-ended three-stage ring oscillator type 5. V_{DD}=3.3 V*

Figure 18 depicts the measured Off-chip transient response of an expanded three-stage ring oscillator. In Table 2 a performance summary of the implemented single-ended three-stage ring oscillators is presented. In this table, the *Frequency* represents the average experimental frequency that is obtained by measuring six oscillators fabricated in six different chips. The *Phase Noise* metric has been obtained indirectly from experimental results (Figure 19) using the procedure shown in [30]. The *Output voltage* and *Power* denotes the amplitude of the generated signal and power consumption (this value does not include the power of the dividers, buffers, pads, etc.) of the ring oscillator, respectively. Finally, the *Coverage area*

represents the area used by the ring in which the generated signal can be distributed through the integrated circuit.

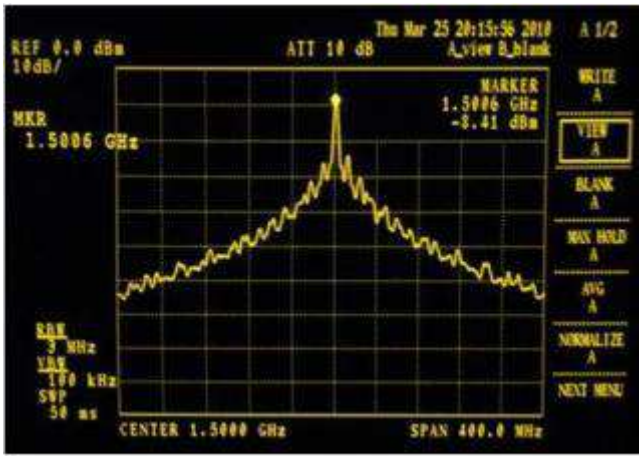


Figure 19. *Power spectral density of the fabricated single-ended three-stage ring oscillator type 5.*

From Figure 17 and Table 2, we can notice that the operating frequency of the ring decreases linearly with the length of interconnection lines used, in accordance with equation (3). For the case of the three-stage ring oscillator implemented using interconnection lines with *l=3000 um*, this oscillator shows the best performance in terms of output voltage, phase noise, and coverage area. However, it has the worst performance in terms of operating frequency and energy efficiency.

Table 2. *Performance summary of single-ended three-stage ring oscillators*

Oscillator type / Parameter	1	2	3	4	5
Interconnection (µm)	70	1000	1500	2000	3000
Frequency (GHz)	2.58	2.14	2.01	1.84	1.500
Phase noise (dBc/Hz) @ 1MHz	-93.06	-95.74	-97.11	-99.53	-102.02
Output voltage V)	3.06	3.12	3.16	3.18	3.19
Power (mW)	2.80	2.96	3.04	3.13	3.32
Coverage area of the ring (mm^2)	0.005	0.56	1.56	2.25	5.06

4.2. Single-ended Three-delay stage oscillators.

Figure 20 shows the layout of the expanded one stage differential VCOs. The signal generated by these oscillators is distributed to the load circuits using interconnection lines of *w=2 µm* and length *l=2.0 mm* implemented in Metal 4. In the case of the expanded three stages multiple-pass differential VCO (Fig. 20c), the delay-stages are interconnected and distributed using interconnection lines of length *l=0.6 mm*. All differential oscillators are designed to simultaneously generate and distribute signals at maximum possible operation frequency over an area of 500 x 500 μm^2.

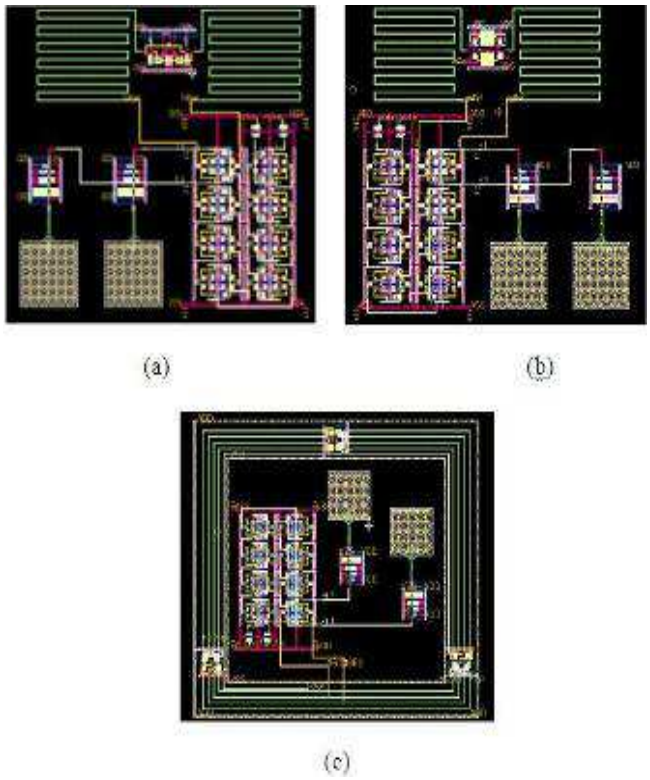
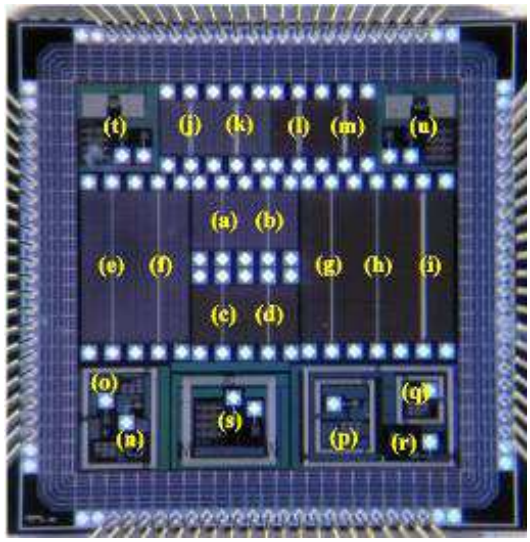
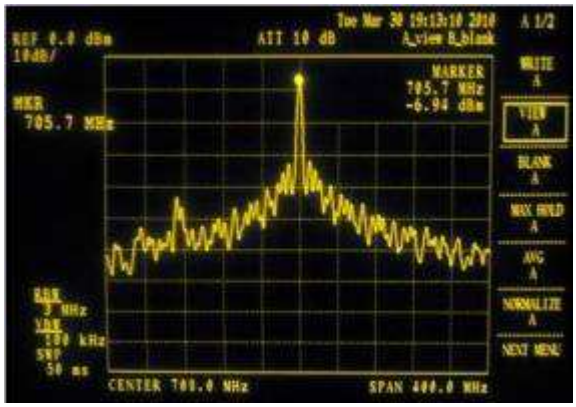


Figure 20. *Layout of the differential expanded ring oscillators: (a) Mostafa, (b) Ahmed, (c) Yalcin*

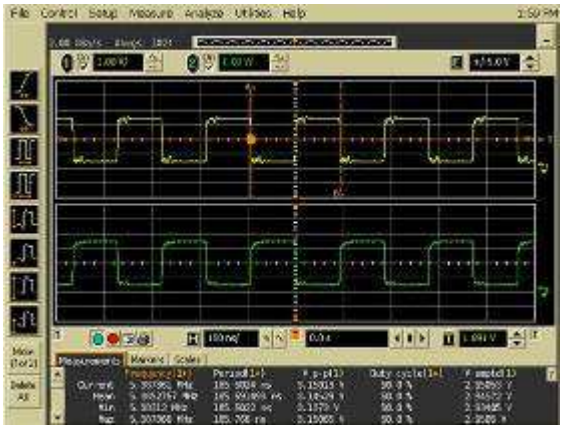


Item	Structure
(a to m)	Interconecction lines
	Single-ended oscillators
(n)	*l=70 µm*
(o)	*l=2000 µm*
(p)	*l=1500 µm*
(q)	*l=1000 µm*
(r)	*l=3000 µm*
	Differential oscillators
(s)	Three stage,*l*=660 µm
(t)	One-stageD-latch,*l*=1800 µm
(u)	One stage,*l*=1200 µm

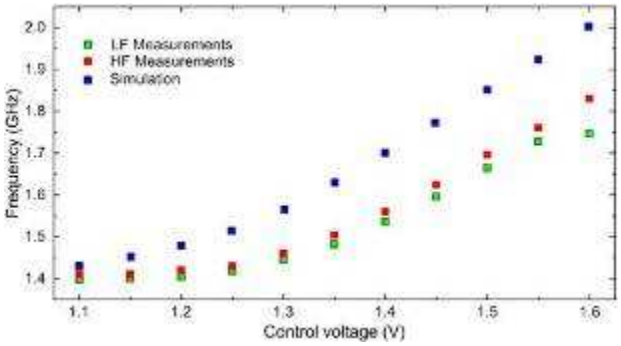
Figure 21. *Microphotograph of the Test chip.*



(a) *Power spectral density: Vc=1.1 V, F= 708 MHz X 2=1.41GHz*



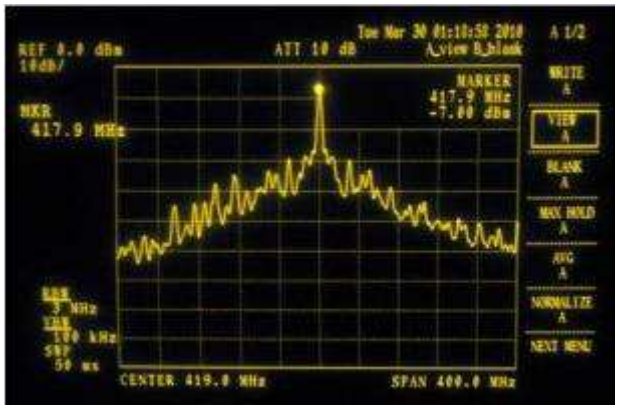
(b) *Transient response: Vc=1.1 V, F= 5.38 MHz X 256=1.38GHz*



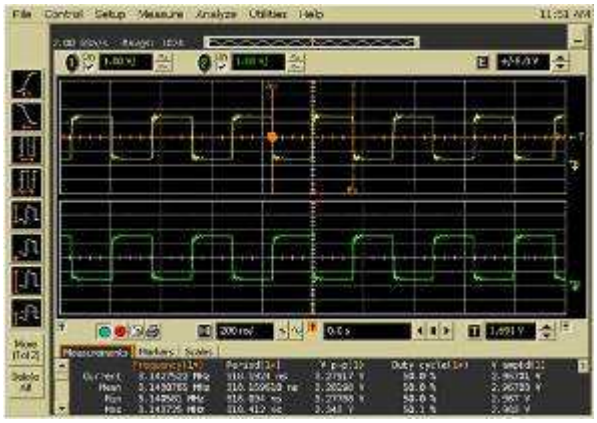
(c) *Frequency vs. control voltage*

Figure 22. *Experimental and simulated measurements of the one stage differential oscillator (Mostafa), V_{DD}=3.3 V, l=2.0 mm.*

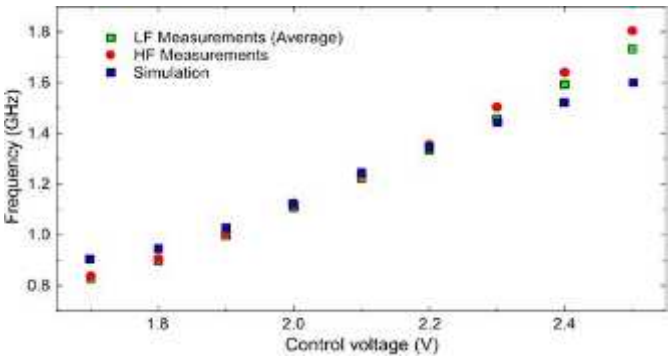
Figure 21 shows de fabricated test chip containing the different oscillators, and other structures. In order to analyze the influence of interconnections in the performance of expanded ring oscillators, several parameters (operation frequency, phase noise, output voltage, power consumption, energy, and coverage area of the implemented oscillators) were simulated and experimentally measured and compared. The measurements are performed on wafer (On-chip) and on package (Off-chip). For the case of the experimental transient response, Off-chip measurements were performed as follow: the high-frequency signal generated by the oscillator is divided by a factor of 2^M , where M is the number of dividers used in the implementation (in this case $M=8$ dividers were used, this way the division factor is 2^8=256. Therefore the off-chip measurements must be multiplied by 256 to obtain the real value (by example see Fig. 22). Then, the signal is fed to the output pad that is responsible to drive the external load. The Off-chip measurements are performed using an Infiniium 54833A Oscilloscope with flexible cables and the corresponding oscilloscope probes.



(a) *Power spectral density: Vc=1.7 V, F= 419 MHz X 2=0.84GHz*



(b) *Transient response: Vc=1.7 V, F= 3.14 MHz X 256=0.80GHz*

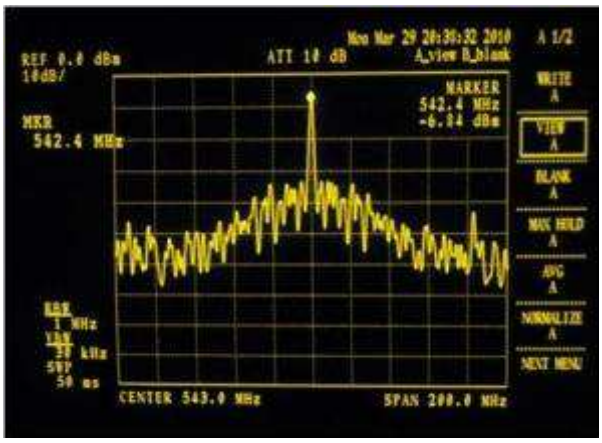


(c) *Frequency vs. control voltage*

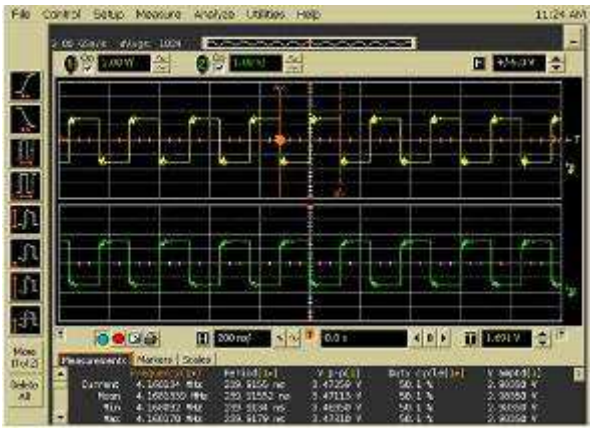
Figure 23. *Experimental and simulated measurements of the one stage D-latch differential oscillator (Ahmed): V_{DD}=3.3 V, l=1.8 mm.*

For experimental phase noise, On-chip measurements,

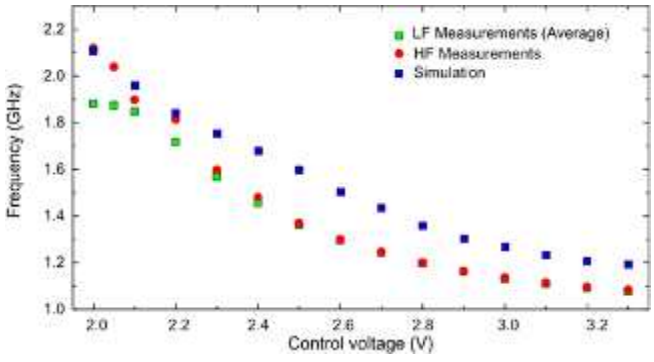
the high-frequency signal generated by the oscillator is divided by a factor *M=2*; then, the divided signal is fed to the high-frequency buffer which is responsible to drive the load associated with the internal pad and the device probe. The On-chip measurements were performed using an Advantest R3265A series spectrum analyzer with a semi-rigid cable and the corresponding on-chip one point probes.



(a) *Power spectral density: Vc=3.3V, F= 543 MHz X 2=1.08GHz*



(b) *Transient response: Vc=3.3 V, F= 4.17 MHz X 256=1.07GHz*



(c) *Frequency vs. control voltage*

Figure 24. *Experimental and simulated measurements of the three-stage multiple-pass differential oscillator (Yalcin):V_{DD}=3.3 V. l=0.66 mm.*

In the Figures 22 to 24 the simulation and experimental results of the fabricated expanded differential oscillators are shown. The power spectrum was measured at the divide-by-two (*M=2*) output of the oscillator. The phase noise of the oscillator was extracted at a 1-MHz offset from a center frequency; this value accounts for the bandwidth of the input low-pass filter of the spectrum analyzer and the division factor. In Table 3 the performance summary of the implemented differential oscillators is given.

In general, from Table 3 and figures 22 to 24, we can see that the simulated and experimental results of the several parameters obtained from the VCO`s show the same behavior.

Table 3. *Performance summary of differntial oscillators*

Oscillator type		Yalcin	Ahmed	Mostafa
Interconnection length (mm)		0.66	1.8	2.0
Frequency (GHz)	Simulation	1.19-2.37	0.90-2.09	1.42-2.07
	Experimental	1.08-2.12	0.83-1.80	1.41-1.82
Tuning range (GHz)	Simulation	1.18	1.19	0.65
	Experimental	1.04	0.97	0.41
Output voltage (V)	Simulation	2.0	1.13	1.15
	Experimental	2.06	1.45	1.18
Power (mW)	Simulation	111	92	20
	Experimental	108	91	17
Energy (pJ)		50.94	50.55	9.34
Phase noise (dBc/Hz)@ 1MHz		-88.18	-93.22	-90.74
Coverage area of ring (μm x μm)		500x500	450x450	500x500

Experimentally the one-stage differential oscillator from Mostafa simultaneously generates and distributes a signal with a maximum operating frequency and output voltage of 1.82 GHz and 1.18 V, respectively. The maximum operating frequency of this oscillator is 14% lower than the maximum frequency of the three-stage multiple-pass oscillator from Yalcin that shows the highest operating frequency (2.12GHz). The one-stage oscillator resulted with the lowest tuning range (0.41GHz) and output voltage (1.18V); however, it has the highest energy efficiency de 9.34 pJ, i.e., has the lowest speed-power product of the three differential oscillators which is one of its main advantages.

The one-stage D-latch oscillator shows a maximum operating frequency and output voltage of 1.80 GHz and 1.45V, respectively. The maximum operating frequency of this oscillator is 15% lower than the maximum frequency of the Yalcin´s oscillator (2.12 GHz); while, its energy efficiency is similar than the multiple-stages differential oscillator (50.5 pJ). Likewise, one of the main advantages of this topology is its wider phase noise (-93.2 dBc/Hz).

Finally, the Yalcin's oscillator has the highest operating frequency (2.12 GHz) and the highest output voltage (2.06 V), as well as a wide tuning range (1.04 GHz), similar to the Ahmed´s oscillator. These characteristics are result of the use of auxiliary feedback loops and saturated stages that allow increasing the operating frequency (even using a larger number of stages) and the output voltage of the generated signal. Nonetheless, due to the high operating

frequency and high power consumption (108 mW), this oscillator is the one with the lowest energy efficiency (50.94 pJ) that represents one of the main disadvantages with respect to the one-stage oscillator from Mostafa.

For the case of phase noise, as can be observed in Table 3, the Ahmed´s oscillator presents the best phase noise performance with a -93.22dBc/Hz at a 1 MHz offset frequency from a 1.44 GHz center frequency.

5. Perspective

Currently, the local resonant oscillators (LC-tank, standing-waves, rotary-waves, etc.) for CMOS technology show better performance characteristics (frequency and phase noise) than non-resonant ring Voltage/Current Controlled Oscillators (VCOs/CCOs); however, implementing inductors with high-quality factor [31] or high-precision transmission lines in a standard CMOS process require more steps of design which are always limited by parasitic effects. Moreover, resonant oscillators generally have a narrow tuning range. Because of the aforementioned, oscillators non-resonant (without inductors) are more attractive due to following characteristics:

Simple topology, high regularity and modularity.

Highly integrables and compatible with CMOS technologies.

They generate frequencies in the GHz range, approximately between 10-20 % of the maximum frequency (f_{max}) of the technology (Fig. 25).

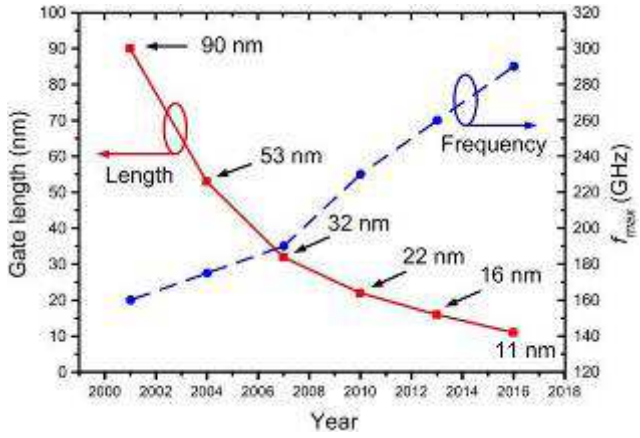


Figure 25. *Minimum length gate and maximum frequency f_{max} in CMOS technology*

Depending on the stages number *N* in the basic ring, signals can be generated with high quadrature and multiple phases.

Because inductors no are required, the area, complexity and cost of implementation are reduced.

The design of the network is simpler and direct, since his design comes down to the optimal design of the basic oscillator and the repetition of the same one.

Because the design of the whole Local Clock Generation and Distribution Network is reduced to the design and optimization of the basic oscillator, its operation frequency is scalable with the technology.

It is observed that the voltage/current-controlled oscillator is the basic building block not only for analogical and digital circuits, but also for the control signal generation and distribution of performance themselves. Especially, the ring oscillators fabricated with MOS transistors only can be easily implemented and integrated in standard CMOS process. This is allowing higher-frequency of operation of the VCOs [23, 24, 32] with the scaling of MOS devices (Fig. 25) [45], even using a higher number of delay-stages (Fig. 26).

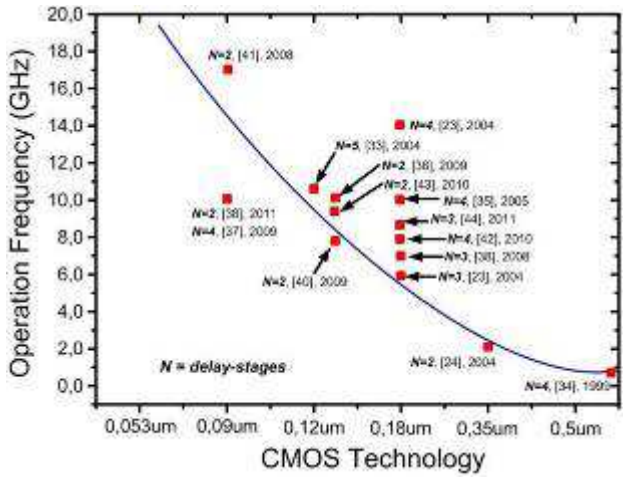


Figure 26*. Operation frequency tendency from ring oscillators found in the open literature*

5. Conclusions

In this work, we have shown that using differential expanded ring oscillators it is possible to generate and distribute high frequency signals on a relatively large area. Despite its high power consumption, the expanded ring VCOs represents an excellent alternative for the design and implementation of non-resonant LCGDN because its many attractive characteristics such as simple topology, high regularity and modularity, high integrability, and compatibility with CMOS technologies.

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