

# Power System Distortions Mitigation Using Switched Filter Compensator

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## To cite this article:

Sahar Gamaa, Abdelazeem Abdelsalam, Almoataz Abdelaziz. Power System Distortions Mitigation Using Switched Filter Compensator. *American Journal of Electrical Power and Energy Systems*. Vol. 5, No. 6, 2016, pp. 76-80. doi: 10.11648/j.epes.20160506.13

**Received:** November 14, 2016; **Accepted:** November 26, 2016; **Published:** January 4, 2017

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**Abstract:** This paper proposes a novel low-cost switched power filter compensator (SFC). This proposed SFC is considered as a new topology of distribution FACTS. The proposed SFC scheme is based on a switching on/off process for connecting /disconnecting double tuned arm filters intermittently with two parallel capacitor-banks. The parallel capacitor-banks are connected at the two sides of series capacitor bank. When the switch is on, the SFC works as a double tuned filter while when the switch is off, the SFC works as series/shunt compensator. The switching process is controlled by a pulsing signal generated from PWM circuit. The modulation control signal of PWM is generated from a multi-loop traditional control. The Matlab Simulink environment is used to validate the ability of SFC to mitigate power quality problems, stabilize the system voltage and enhance the system power factor. The results show that the effectiveness of SFC to solve the system quality problems. This novel topology might be extended to be used with renewable energy resources interconnection and microgrids performance applications.

**Keywords:** Power Quality, D-FACTS, Switched Filter Compensator

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## 1. Introduction

A power quality issue is known as any problem reveals in the waveform voltage and current or in frequency value that causes a malfunction of protection devices or mal operation of equipment. The PQ problems is categorized into many issues such as voltage transient, sag, swell, interruption, voltage unbalance and harmonics [1]. The cause of the bad PQ result from increasing use of many equipment, such as solid state switching devices, nonlinear and power electronically switched loads, unbalanced power systems, lighting controls, computer and data processing equipment [2].

The improvement of the power quality is of great important at the load side when the production processes get more complicated and require a bigger liability level. This improvement includes aims to provide the energy without interruption, without harmonic distortion and with tension

regulation between very narrow margins. The devices that can fulfill the requirements of this improvement are the custom power devices; a concept that could be included among the FACTS, but they are different to them because of their final use [3]. With the development of power electronic devices, customized power devices have become possible to play an important role in emerging deregulated power systems with versatile new control capabilities [4].

In general, custom power or distribution FACTS (D-FACTS) devices are used for distribution system control while FACTS devices are used in transmission system control. The D-FACTS devices that include distribution synchronous static compensator (DSTATCOM), dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC) have been developed for improving power quality, stability and reliability of distribution systems [5-7].

Advanced control and improved semiconductor switching of these devices have reached a new era for power quality

mitigation. The D-FACTS devices have been developed for mitigating specific power quality problems. Where DSTATCOM which is a shunt compensator is used for reactive power and voltage sag compensation [8, 9], DVR which acts as a series compensator is used for voltage sag compensation [10, 11] while the unified power quality conditioner (UPQC) contains both a shunt and a series device that are joined together at a common dc bus [12].

On the other hand, to reduce quasi-steady harmonic distortion, passive, switched/modulated and active filter compensation techniques can be implemented. Passive filters have the drawback of bulky size, component aging, resonance and limited fixed compensation and filtering performance. These provide either over or under-compensation of harmonics, whenever a dynamic load change occurs [13, 14]. Hence, active compensation known as active power filter (APF) is preferred over passive compensation. APF's are an up-to-date solution to power quality problems, which allow the compensation of current harmonics and imbalance together with power factor improvement [15, 16].

A new kind of series/shunt power filter compensators which can mitigate a wider range of power quality problems have been developed [17- 26].

In this paper, a novel low-cost switched filter compensator is presented and validated for power quality enhancement and power factor improvement with an adequate voltage stabilization. The proposed D-FACTS scheme is based on a switching on/off process between two shunt capacitor banks and two parallel tuned arm filter. The switching process is achieved by a pulse signal generated from pulse-width modulation (PWM) switching. The proportional-integral-derivative (PID) controller which is used to modulate the PWM is driven by an error signal generated from a multi-loop traditional controller. The SFC scheme has been fully validated for effective harmonic mitigation, voltage stabilization and power factor correction using the Matlab/Simulink software environment.

## 2. The Proposed Switched Filter

The proposed SFC scheme, shown in Fig. 1, is a combination of one series capacitor bank and two shunt capacitor banks connected with each other then they are connected to two parallel tuned arm power filters through an intermittent switch (SA). The switch (SA) is controlled by a pulse signal P1 that is generated by PWM, as shown in Fig. 2. The variable SFC filter topology can be changed by the pulse signal P1 as follows:

Case 1: If P1 is low, the switch SA will be opened and the combined shunt and series capacitors will provide the required shunt and series reactive power compensation to the AC distribution system

Case 2: If P1 is high, the switch SA will be closed and the shunt capacitors will make a double tuned filter with two arm filters

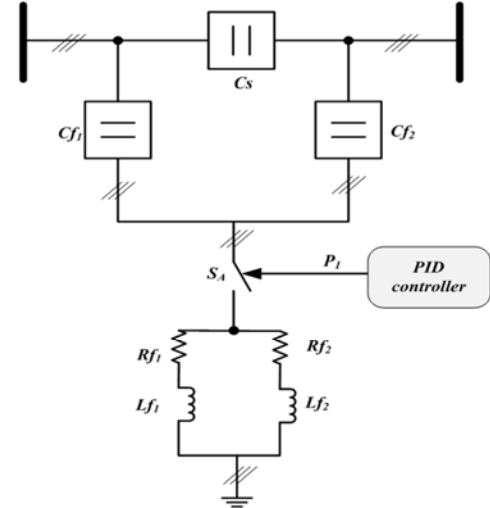


Figure 1. The proposed scheme of the switched filter compensator.

## 3. Controller Design

In order to reduce the harmonics, improve the power factor and stabilize the buses voltage using the proposed SFC, a traditional dynamic control based on PID controller driven by a multi-loop error. The output of PID,  $V_g$ , is the modulating control signal to the PWM switching block as shown in Fig. 2. The global error ( $e_g$ ) is the summation of a multi-loop individual errors including voltage stability and current limiting errors.

The voltage stability error is:

$$e_{V_2} = V_{2ref} - V_2 \left( \frac{1}{1+ST_1} \right) \quad (1)$$

and current limiting error is:

$$e_{I_2} = I_2 \left( \frac{1}{1+ST_1} \right) \left( 1 - \frac{1}{1+ST_2} \right) \quad (2)$$

The global error is:

$$e_g = e_{V_2} + e_{I_2} \quad (3)$$

The modulating signal of the PWM,  $V_g$ , is adapted to minimize this global error as shown in eq. (4).

$$V_g(t) = K_p e_g(t) + K_i \int_0^t e_g(t) dt + K_d \frac{d(e_g(t))}{dt} \quad (4)$$

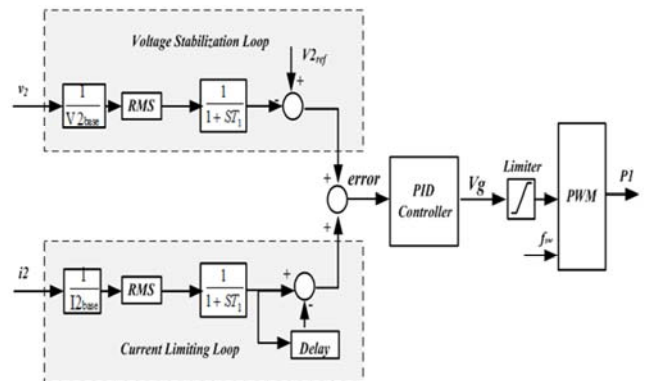


Figure 2. The used controller of the proposed SFC scheme.

## 4. Simulation Results

### 4.1. The AC System Configuration

The single line diagram of the studied AC system is shown in Fig. 3. A hybrid load comprises a linear load, a converter type non-linear load and induction motor load are connected to the AC network through 25/4.16 kV step-down. 10 km feeder. The detailed parameters of the system are given in the Appendix.

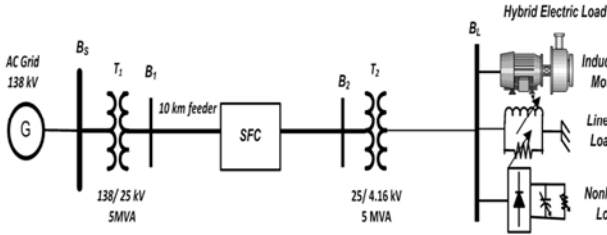


Figure 3. The single line diagram of the sample study distribution system with the proposed SFC.

### 4.2. Results and Discussion

The digital simulation results using Matlab Simulink environment for the proposed SFC under normal operating condition are shown in Figs. 4- 8. The dynamic response of the voltage, current, reactive power, power factor and power losses at the source bus,  $B_s$ , and at the load,  $B_L$ , are monitored in the test system without and with inserting the proposed SFC. In Fig. 4, the voltage at the load bus is enhanced to 0.95 pu while there is no change at the source bus. The reactive power at the source bus decreased and this increases the power factor from 0.938 to 0.99, as shown in Fig. 7. While the reduction of the reactive power at the load bus is very small, as shown in Fig. 6, and this leads to a very small enhancement in the power factor, as shown in Fig. 7.

The power factor values of the system buses without and with inserting the proposed SFC are monitored and recorded in Table 1.

The system power losses are calculated and are depicted in Fig. 8. As shown in the figure, the power losses are reduced from 0.03 pu to 0.004 pu with inserting the SFC. And the percentage reduction of loss in the power equals to 86 %.

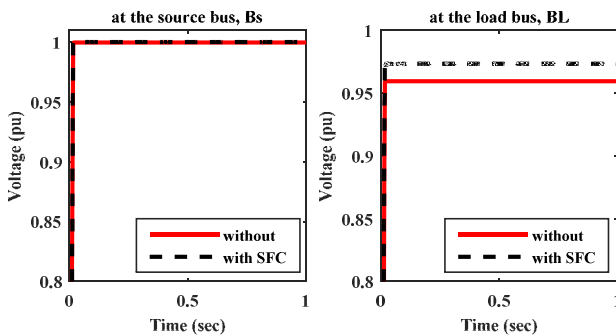


Figure 4. The rms value of the voltage at the source and load buses.

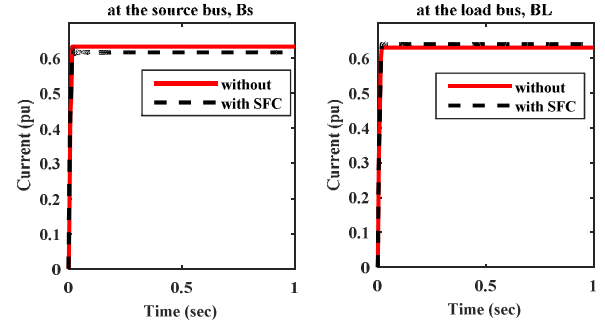


Figure 5. The rms value of the current at the source and load buses.

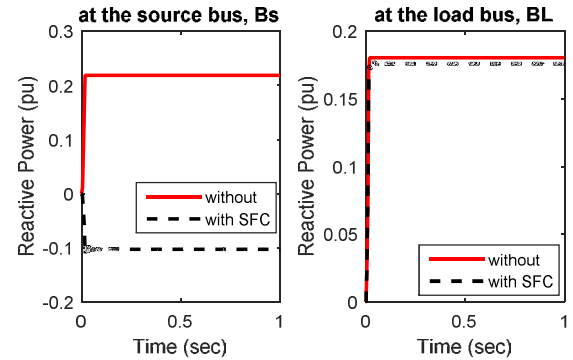


Figure 6. The reactive power at the source and load buses.

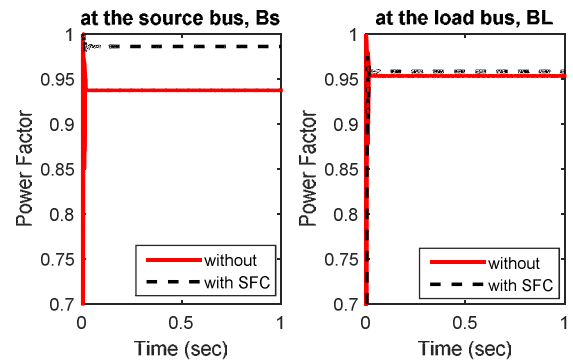


Figure 7. The power factor at the source and load buses.

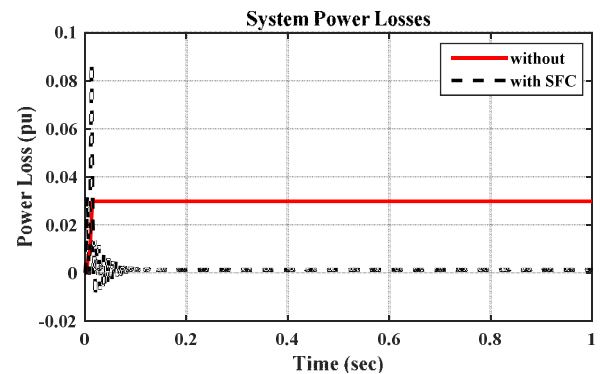


Figure 8. The total power losses of the system without and with SFC.

Table 1. The Power Factor Values At All AC Buses.

	Source, $B_s$ , bus	$B1$ bus	$B2$ bus	Load, $B_L$ bus
Without SFC	0.938	0.943	0.948	0.952
With SFC	0.988	0.985	0.958	0.963

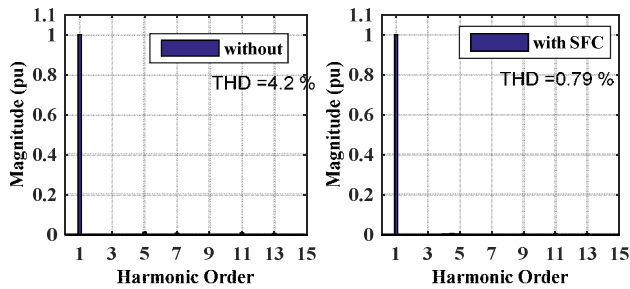


Figure 9. The frequency spectrum of the voltage waveform at B1 bus.

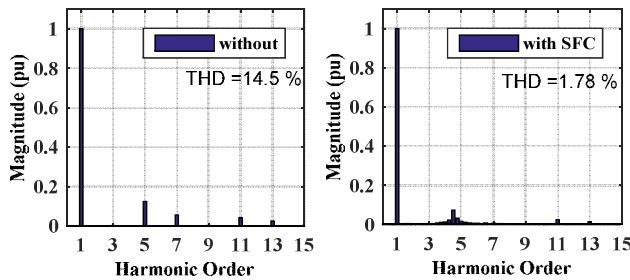


Figure 10. The frequency spectrum of the current waveform at B1 bus.

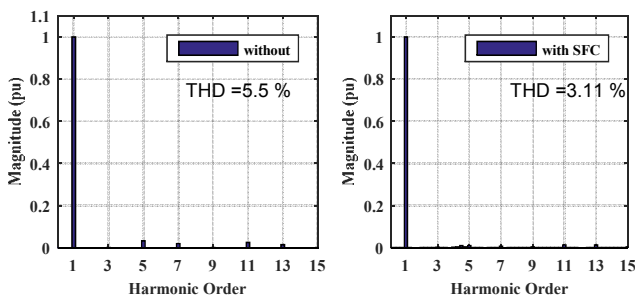


Figure 11. The frequency spectrum of the voltage waveform at B2 bus.

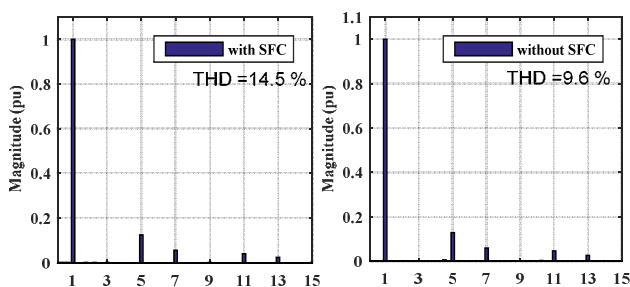


Figure 12. The frequency spectrum of the current waveform at B2 bus.

The harmonic spectra of the voltage and current waveforms of buses at the two sides of the SFC,  $B_1$  and  $B_2$ , are shown in Figs. 9-12. Also The voltage and current harmonic analysis in term of the total harmonic distortion (THD) at all the system buses are calculated and are summarized in Table 2. It is obvious that the voltage harmonics at the source bus are significantly reduced to a level within the limit set by the IEEE Std. 519-1992 (IEEE, 1992) regarding the THD of bus voltage at low voltage system (less than 69 kV) [27]. Also the THD of current waveform at each bus is decreased.

Table 2. The THD values of voltage and current waveforms at all AC buses.

	% THD of the voltage waveform		% THD of the current waveform	
	Without	With SFC	Without	With SFC
Source, Bs, bus	3.07	1.5	14.56	4.20
B1 bus	4.2	0.79	14.5	1.78
B2 bus	5.5	3.11	14.5	9.6
Load, BL <sub>2</sub> , bus	7.4	4.7	14.6	14.6

## 5. Conclusions

This paper presents a novel D-FACTS scheme based on the SFC for harmonic mitigation, voltage stabilization, efficient energy utilization and power factor correction. The novel SFC is controlled by PID controller to regulate the modulating control signal to the PWM switching block. The SFC scheme has been fully validated for effective harmonic mitigation, voltage stabilization, efficient energy utilization and power factor correction using Matlab/Simulink software environment. This novel scheme can also be extended to be used with renewable energy resources interface and microgrids performance applications

## Appendix

- AC Grid:  
 $V = 138$  KV,  $X/R=10$ , SC. level=5 GVA.
- Transformer  $T_1$ : 5 MVA, 138/25 kV.
- Transformer  $T_2$ : 5 MVA, 25/4.16 kV.
- Hybrid AC Load:  
 Linear load: 2 MVA, 0.85 lag pf.  
 Non-linear load: 1.5 MVA.  
 Induction motor: 3phase, 1.5 MVA, no of poles=4,  
 Stator resistance and leakage inductance (pu)  
 $R_s=0.01965$ ,  $L_s=0.0397$   
 Rotor resistance and leakage inductance (pu)  
 $R_r = 0.01909$ ,  $L_r=0.0397$   
 Mutual inductance  $L_m$  (pu) =1.354
- 10 Km Distribution Feeder:  
 $V_{L-L} = 25$  kV,  $R/km=0.35 \Omega$ ,  $X/km=0.4 \Omega$
- The proposed SFC:  
 $C_s/\text{phase} = 100 \mu\text{F}$ ,  $C_{f1}/\text{phase} = C_{f2}/\text{phase} = 500 \mu\text{F}$ ,  
 $R_{f1} = R_{f2} = 0.05 \Omega$ ,  $L_{f1} = 28$  mH and  $L_{f2} = 65$  mH
- PID Controller Gains:  $K_p=1$ ,  $K_i=0.5$ ,  $K_d=0.02$ ,
- PWM Frequency:  $f_s=1750$  Hz.

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