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Research Article

Optimized Three Bit Counter Employing T Flip-Flop in Quantum-Dot Cellular Automata Technology

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Abstract

Finding new efficient low-cost methods to use CMOS technology is one of the main topics in this area due to the physical limitations of the present methods. The researchers are looking to find new solutions to overcome VLSI problems such as large area, high power consumption, low speed, and electrical current issues. Quantum-dot cellular automata is a new nano-scale technology that has overcome the limits of metal oxide technology and is considered as an advanced method in digital circuit designs. QCA has attracted the attention of many researchers due to its special features such as power consumption, high-speed computing operations, and small dimensions. Besides, the counter is a module that has wide applications in digital systems. In this study, an optimized counter has been proposed in Quantum-dot cellular automata which has utilized T Flip-Flop and improved the cell number and area parameters. The design of the proposed circuit has employed 108 cells. The simulation results of the circuit show 0.1 μm^2 of area occupation. Also, the delay of circuit is 4.25 clock periods. This design has improved the cell number and area by 22% and 39%, respectively. The power or Complexity has reduced by 22% compare to the best prior design.

Keywords

Digital Circuit Design, Quantum-Dot Cellular Automata, T Flip-Flop, Three Bit Counter

1. Introduction

In 1965, Moore has predicted that the number of transistors on a chip would be doubled every 18 to 24 months. According to the predictions, the transistor size will be reached to 5 nm in 2022. However, due to the limitations in complementary metal oxide semiconductor (CMOS) technology, it would not attain smaller sizes [1, 2]. On the other hand, due to encountered problems in this technology such as: high noise absorption, high power consumption, the effect of short circuit and leakage current, the researchers are looking for a technology which is more efficient in terms of power consumption, delay, and area [3, 4]. A new technologies is Quantum-dot cellular automata (QCA) which is provided by Lent in 1993 [5, 6]. In this technology, the polarized states are interpreted as logic levels and quantum dot cell [7]. The majority gate and the inverter are the the most important components which are utilized in the QCA designs [8].

One of the advantages of the QCA is the elimination of current which causes improvement in speed and area of designs, and introduces the researchers a new field for reduction of the area and delay. To this aim, yang et al. have implemented a 3-bit counter based on JK flip-flops that consisted of 616 cells in 1.2 μm^2 area. The delay of their design were 5

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clock periods, and it don't have any significant strengths [9]. Bhavani et al. proposed a counter by 3 T flip-flops consisted of 244 cells and 0.346 μm^2 of area. The delay was 4.25 clock periods. According to the mentioned parameters, there is no advantage in the design except an inverter that intercepts signals attenuation [10]. A 3-bits T flip-flop counter has been designed using T flip-flop by Angizi et al which the cells of this design is 238. The area and delay of this design are 0.36 μm^2 and 4.25 clocks, respectively, which didn't provide significant improvement [11]. Abutaleb [12] has presented a D Flip-Flops counter that includes 196 cells and its area and delay were 0.218 μm^2 and 2 clock periods, respectively. Amirzadeh and et al presented a counter utilizing D flip-flop that had 174 cells and its area was 0.194 μm^2. The delay for mentioned counter were 3 clock periods [13]. A 3-bits counter is proposed by Ali Majeed and et al [14] that is best. it includes 140 cells, the area is 0.16 μm^2 and the delay is 2 clock cycles. This circuit area is the best in comparison with the previous designs. Also, this design has the less delay similar to the design introduced by Amirzadeh et al. and Abutaleb et al.

In continuous of the paper, the following outlines are presented: the QCA review and its clocking are presented in section 2. In section 3 the proposed counter is introduced. The simulation results will be discussed in section 4 and the energy will be provided in section 5 using QCA Designer-E software. Finally and in section 6, the paper is concluded.

2. QCA Review

In electronic, the QCA is employed for the design of nanoscale digital circuits. There are four holes for 2 electrons in QCA and are placed in a square pattern [15, 16]. The electrons can move freely in the holes. In general, due to the electrostatic repulsion between the electrons, expressed in Eq (1), the electrons will fill the diagonal of the square [15]. Since the square has two diagonals, the electrons can form two positions which are termed as "+1" and "-1" poles. These poles can be translated as '1' and '0' logics in digital circuit designs [17, 18]. Figure 1 shows the QCA cell and Eq (2) represents the polarity calculation of the cell [3].

$$F = \mathrm{k}\frac{(q_1)*(q_2)}{r^2} \quad (1)$$

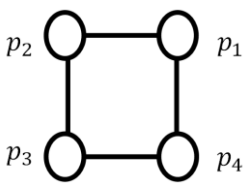

Figure 1. *Representation of the QCA cell.*

$$\text{Polarity} = \frac{(p_1+p_3)-(p_2+p_4)}{p_1+p_2+p_3+p_4} \quad (2)$$

As depicted in Figure 2, the QCA can has 90 and 45 degree phases and both phases have been employed for the present design. The width and length of each cell is 18 nm and the area of the cell is 18×18 nm^2. Also, the interval of the adjacent cells is 2 nm [12].

Figure 2. *Electron arrangement for 45 degree phase 90 degree phase.*

As shown in Figure 3, the electrostatic repulsion of two adjacent cells can change the positions of electrons in the cells and rearranged them to the minimum repulsion force. Therefore, an array of adjacent cells can transfer digital logic as a wire [19-20]

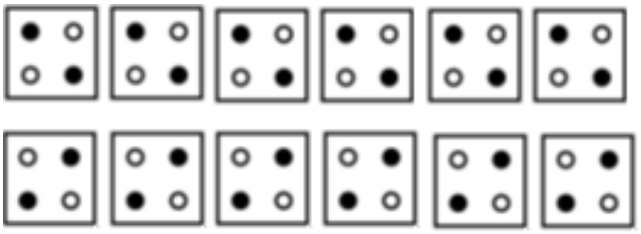

Figure 3. *Formation of a wire using quantum dot cells.*

A clock signals in the QCA can control the electron transitions and causes synchronization in various parts of the circuit. As shown in figure 4 [19], there are four clocks in the QCA that are named as clock 0, clock 1, clock 2 and clock 3 and are displayed by green, purple, blue and white colors. Each clock is consists of four phases witch are named as 'switch', 'hold', 'release', and 'relax'. Figure 5 presents the QCA clocks and the phase difference of two adjacent clocks which is $\frac{\pi}{2}$. More discussion about the clocks can be found in [4, 21-24].

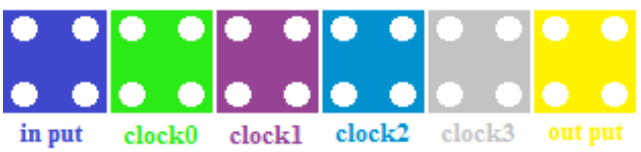

Figure 4. *Color of input, output and clock cells.*

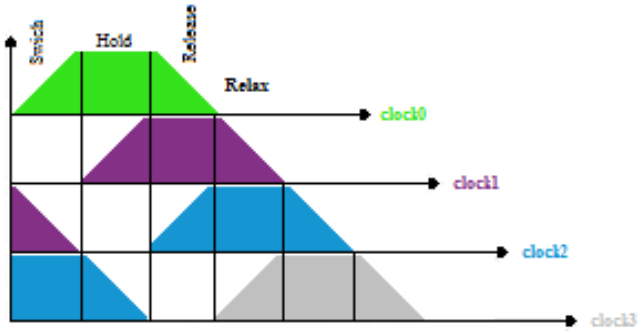

Figure 5. Phase plots in each clock.

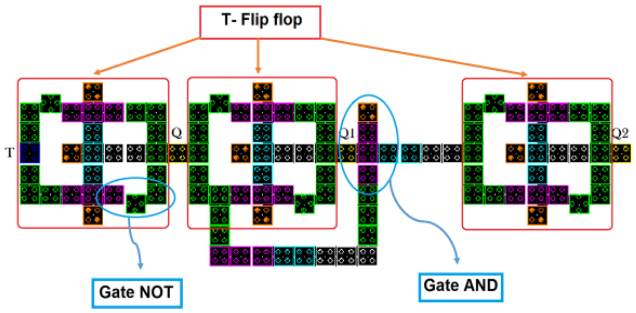

Figure 7. The structure of the proposed 3 bit counter.

3. Proposed Design

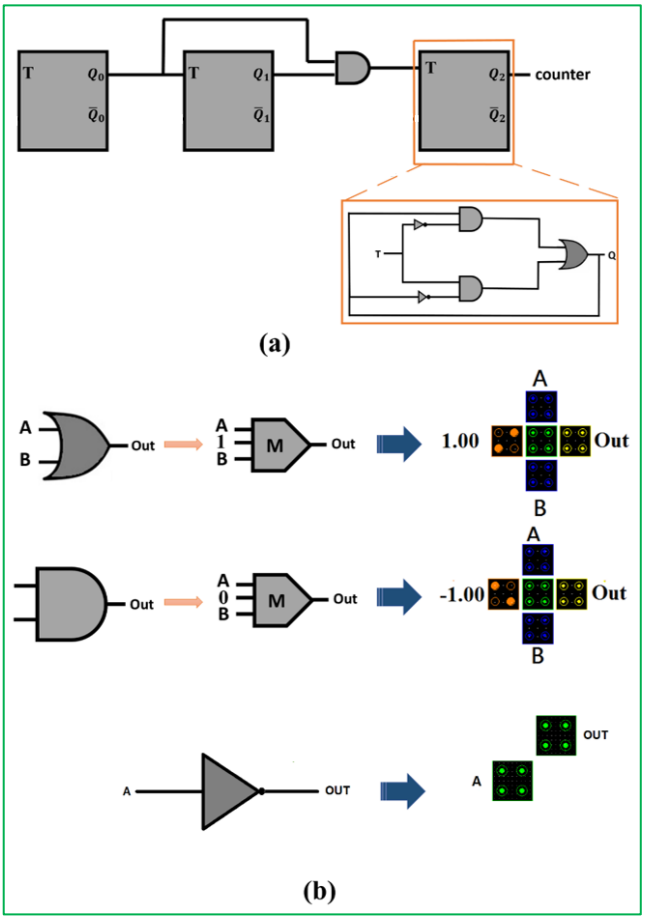

Figure 6. (a) Block diagram of 3-bits counter using T-flip flop. (b) Design of 'AND' and 'OR' gates.

In this paper, a 3 bit counter has been proposed in QCA technology utilizing T-flip flop. The block diagram of the counter and its internal structure has been depicted in Figure 6(a). Each block of the T flip-flop is consists of two inverter, two AND gates and one OR gate [25]. The proposed circuit has utilized the circuits for the "AND" and "OR" gates which are shown in Figure 6 (b). The whole structure of the proposed 3 bit counter is illustrated in Figure 7. As seen, the counter consist of 108 cells and has 0.1 μm^2 area.

The current circuit has improved the design in several steps. The first step is applied to the NOT gates in order to reduce the cells number. As seen, the NOT gates included 3 cells which cause enhancement in the polarity as an advantage in the comparison to previous designs. In the second step, the length of the wires are reduced that causes less cells in the design, and in the third step, the majority gates were connected without any intermediary. In the third step and during the design process, it should be attention that the input clock must be placed after (or before) the majority gate to avoid circuit performance reduction. Since the number of horizontal and vertical cells of the proposed counter has been decreased, it is expected that the area and consumed power of the design are decreased. In the next section, we will discuss on the simulation results of the circuit and the improvement in the mentioned parameters.

4. Simulation Results and Discussion

The proposed counter has been simulated using "QCA-designer" tool. The output waveforms of clock and the output signals have been illustrated in Figure 8. As seen, the circuit operates correctly and the correct numbers are produced by every clock period.

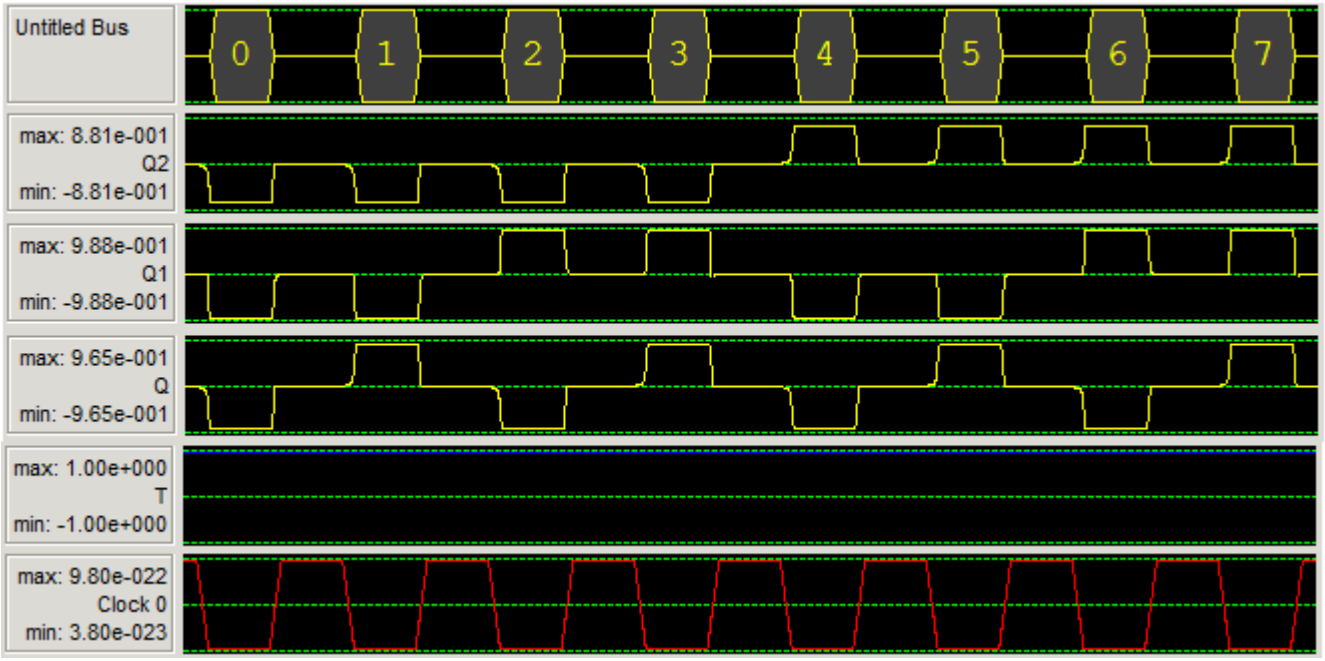

Figure 8. *Simulation of the proposed 3 bit counter.*

Figure 9(a) illustrates the cell number of the proposed design in comparison with the previous deigns. As depicted, the cells number of the proposed circuit is 108 which is lower than all the prior works. The comparison of the occupied area have been depicted in Figure 9(b).

The complexity is equal to the cell numbers and is related to the power as expressed in equation 3:

$$complexity \equiv power \tag{3}$$

The area of our design is 0.1 μm^2 which is lower than the minimum occupied area in the previous studies.

Table 1 shows the simulation results of the proposed counter and the prior works in terms of several parameters. As illustrated in Table1, the occupied area by the circuit has experienced 39% improvement in comparison with the best previous works (0.165 μm^2). Besides the mentioned optimizations, the circuit delay is increased which is a disadvantage of our design. However, the area and other parameters such as complexity are optimized. It is seen in Table 1 that the complexity of circuit, which is equal to 108, has been improved as 22% rather than the best previous design.

Table 1. *Comparison of the proposed design with the previous studies.*

Percent of improvement [14]	Proposed	[14]	[13]	[12]	[11]	[10]	[9]	Measurement metrics
22%	108	140	174	196	238	244	616	Cell Count (cell)
39%	0.1	0.165	0.194	0.218	0.36	0.346	1.2	Area (μm^2)
0%	4.25	2	3	2	4.25	4.25	5	Delay (clock)
22%	108	140	174	196	238	244	616	Complexity (cell)

A parameters which is serious in QCA, is the consumed energy. “QCA designer-E” is a tool which is employed for power measurement [26]. This tool has 2 simulator engines. We employed “Coherence Vector (W/ Energy)” simulator engine in this study. The comparison of total energy dissipation, and the average value of energy dissipation per cycle shows reduction in these two parameters in our study. The simulation results comparison of energies are presented in Table 2. As seen, the total energy dissipated in the proposed scheme is 2.61 eV and has been improved by 23% compare to the best previous design (3.39 eV).

Table 2. The comparison of energies.

Design	Average energy dissipation per cycle (Avg-Ebath)	Total energy dissipation (Sum-Ebath)	Our circuit improvement
[9]	23.72 e-0.03	23.53 e-0.02	89%
[10]	6.84 e-0.03	7.53 e-0.02	65%
[11]	6.03 e-0.03	6.63 e-0.02	60%
[12]	5.34 e-0.03	5.87 e-0.02	55%
[13]	3.08 e-0.03	3.39 e-0.02	23%
[14]	3.39 e-0.03	3.73 e-0.02	30%
[proposed]	2.37 e-0.03	2.61 e-0.02	--------

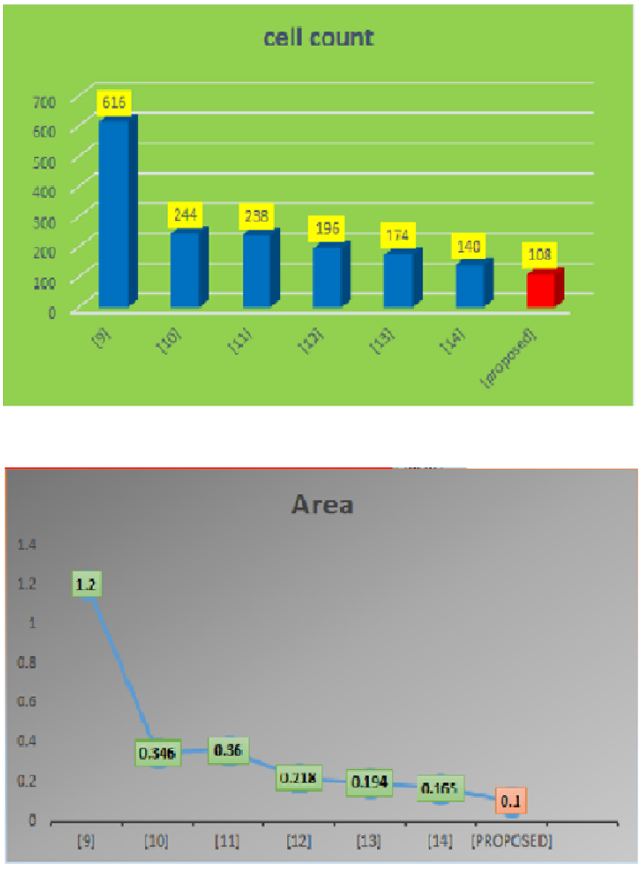

Figure 9. (a) Comparison of the proposed circuit cells number with the previous researches. (b) area of our study and the previous researches.

5. Power Dissipation Analysis

Also, the average energy dissipation per cycle for this counter is 2.37 eV which is lower than the minimum value of average dissipation energy in the previous studies (3.08 eV).

6. Conclusion

A 3-bits counter employing T-flip flop was introduced in this paper. The proposed design has been improved from the aspect of cell number, area and complexity. The block diagram of the counter was determined and the circuit was drawn by the QCA cells. Moreover, in this design, an inverter has been chosen as an efficient inverter in comparison with the previous ones from polarity aspect. Also, the modifications applied in this design caused the increment of energy as 23% which resulted to the more efficient design.

Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
QCA	Quantum-dot Cellular Automata
P	Polarization

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Conflicts of Interest

The authors declare no conflicts of interest.

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